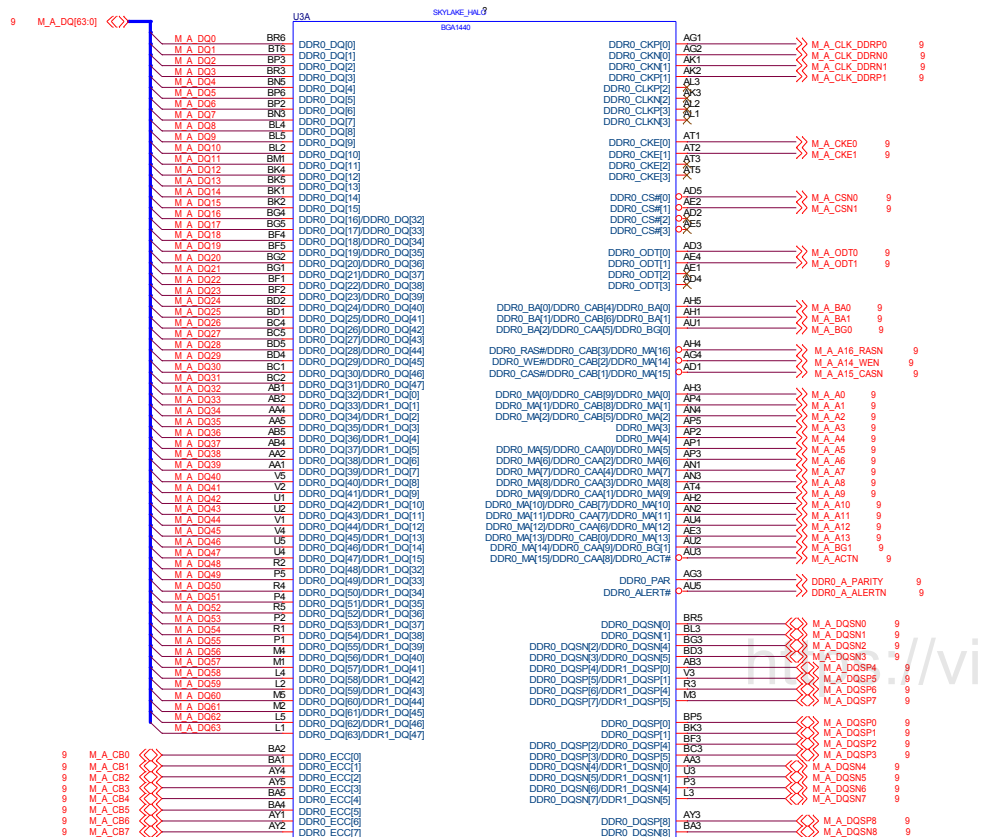
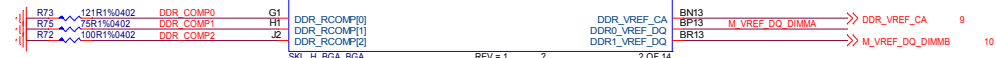
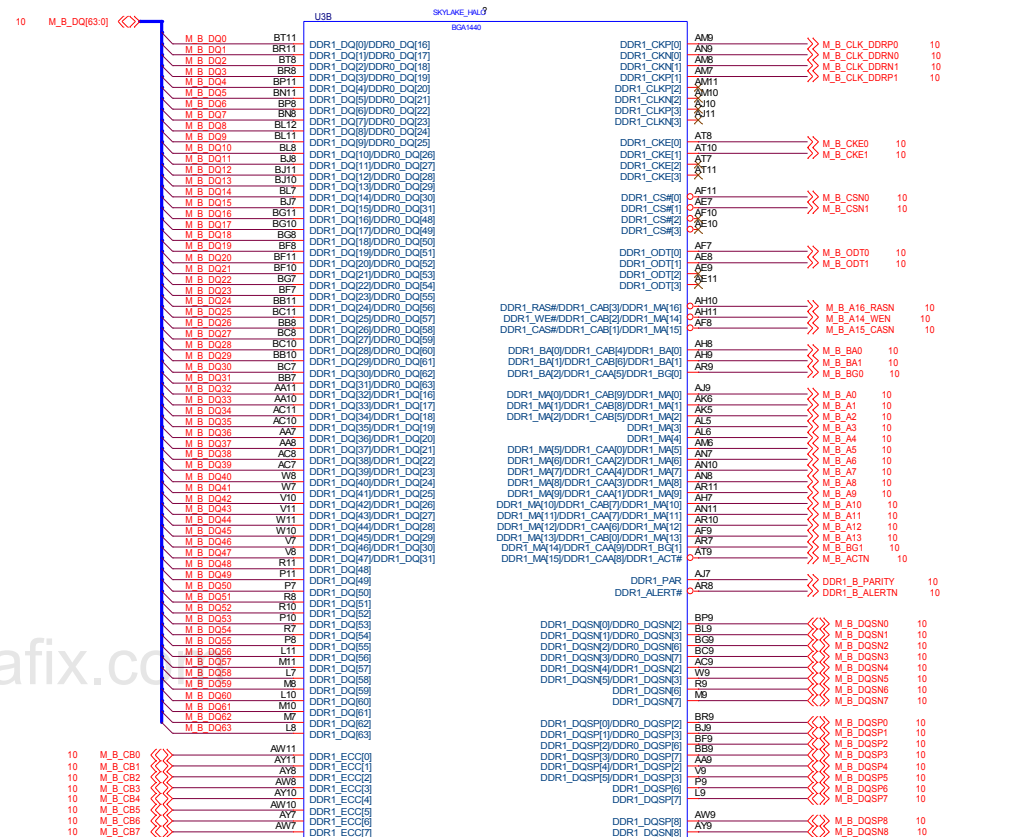
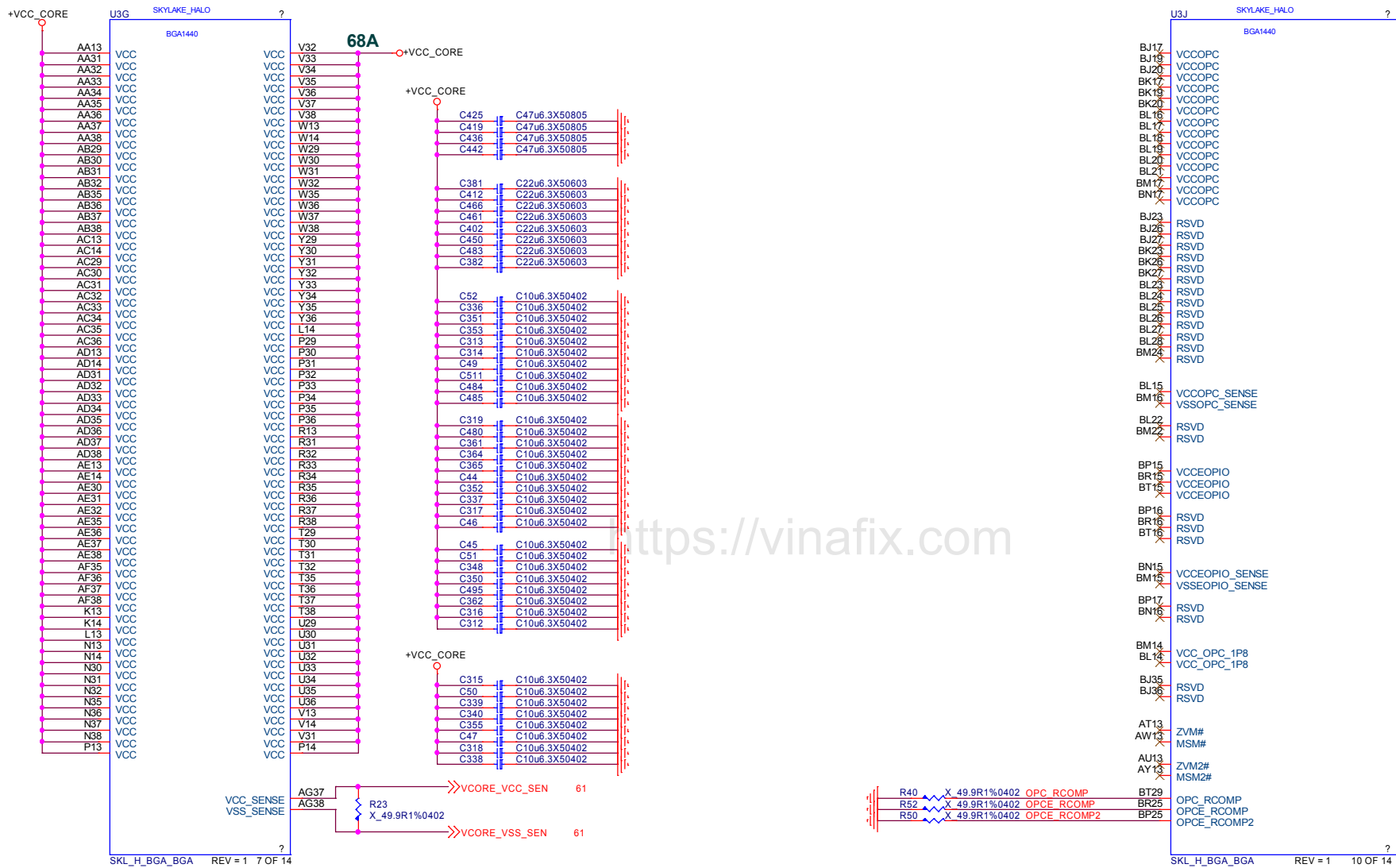


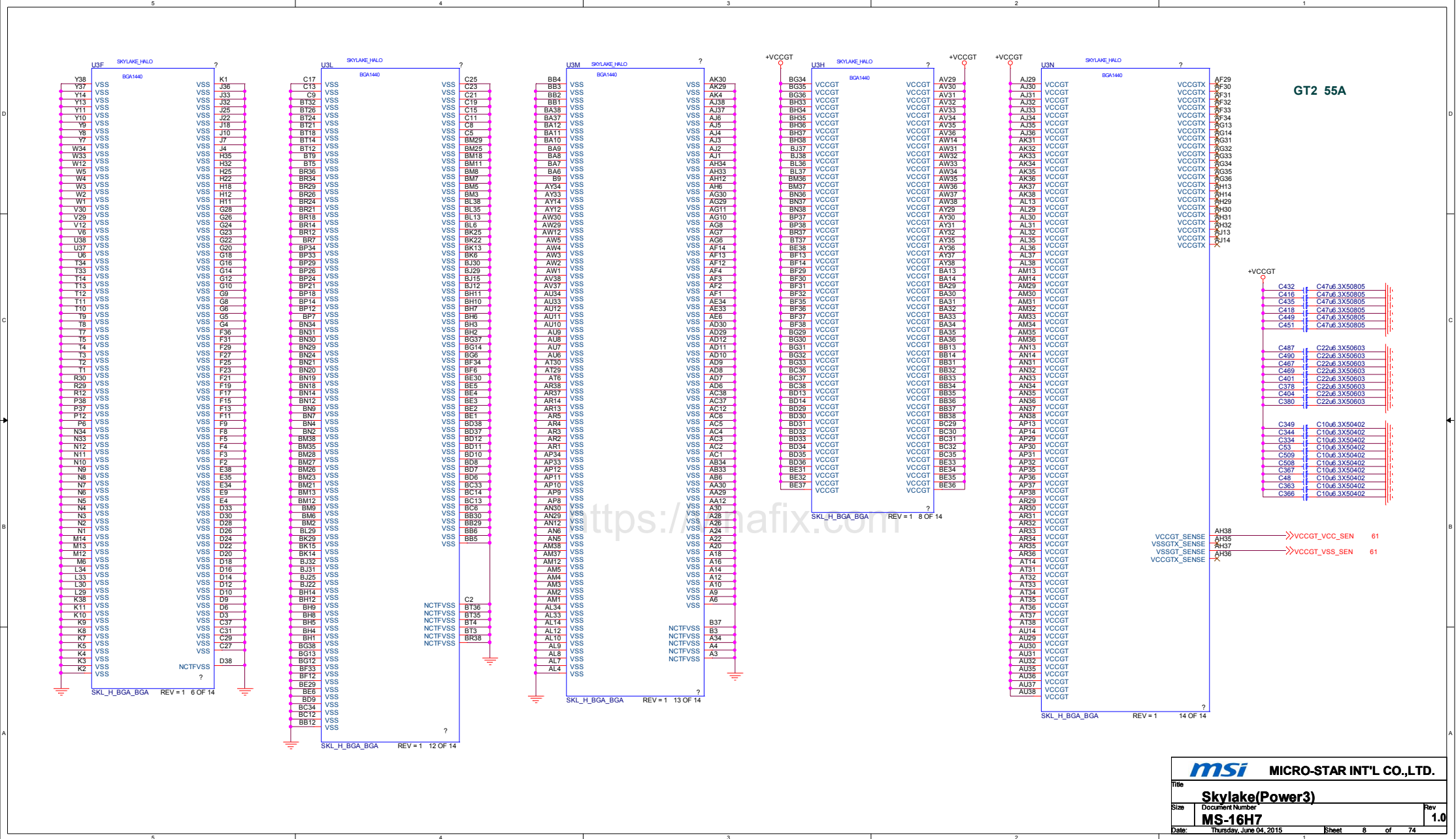
DDR Channel A



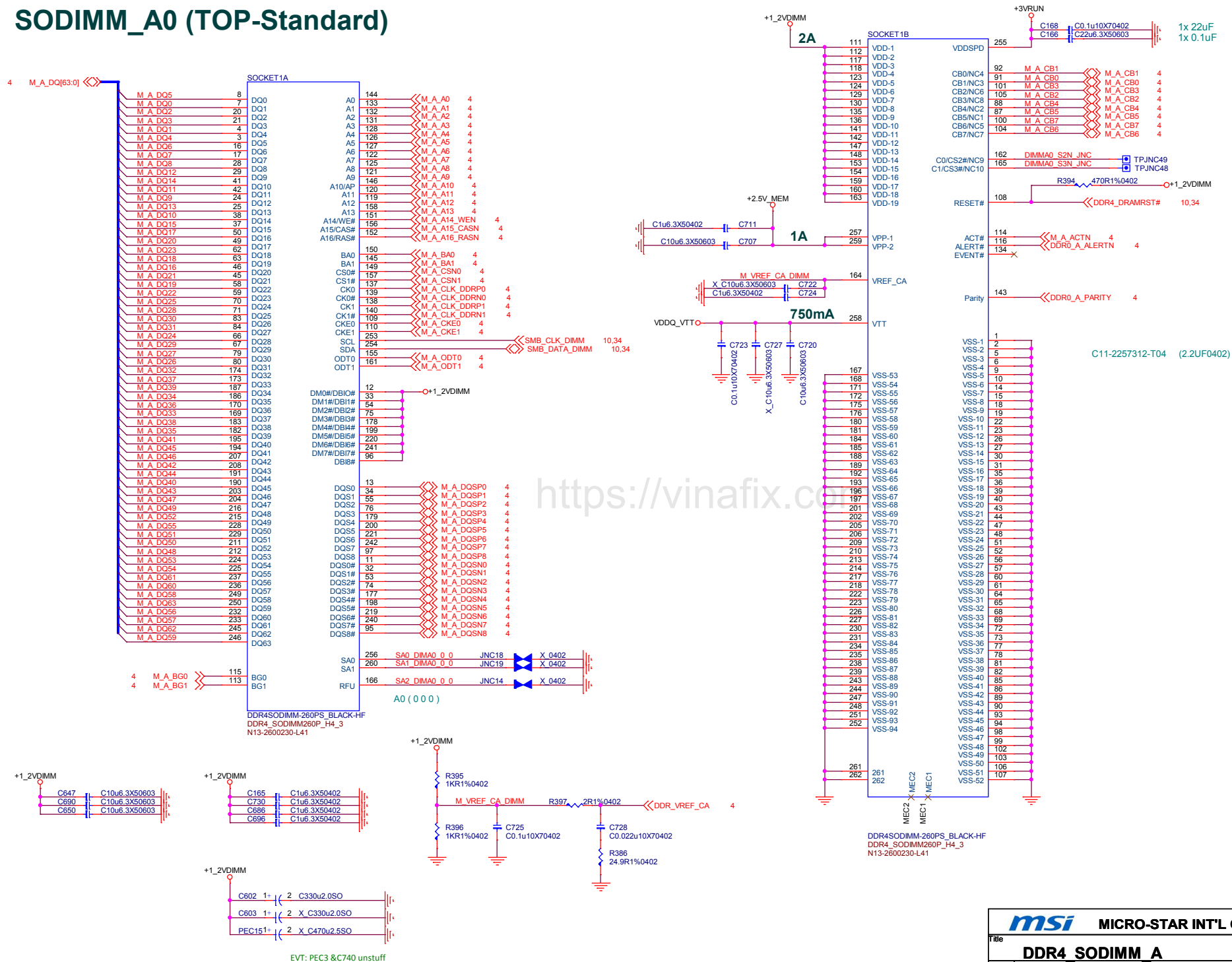
DDR Channel B



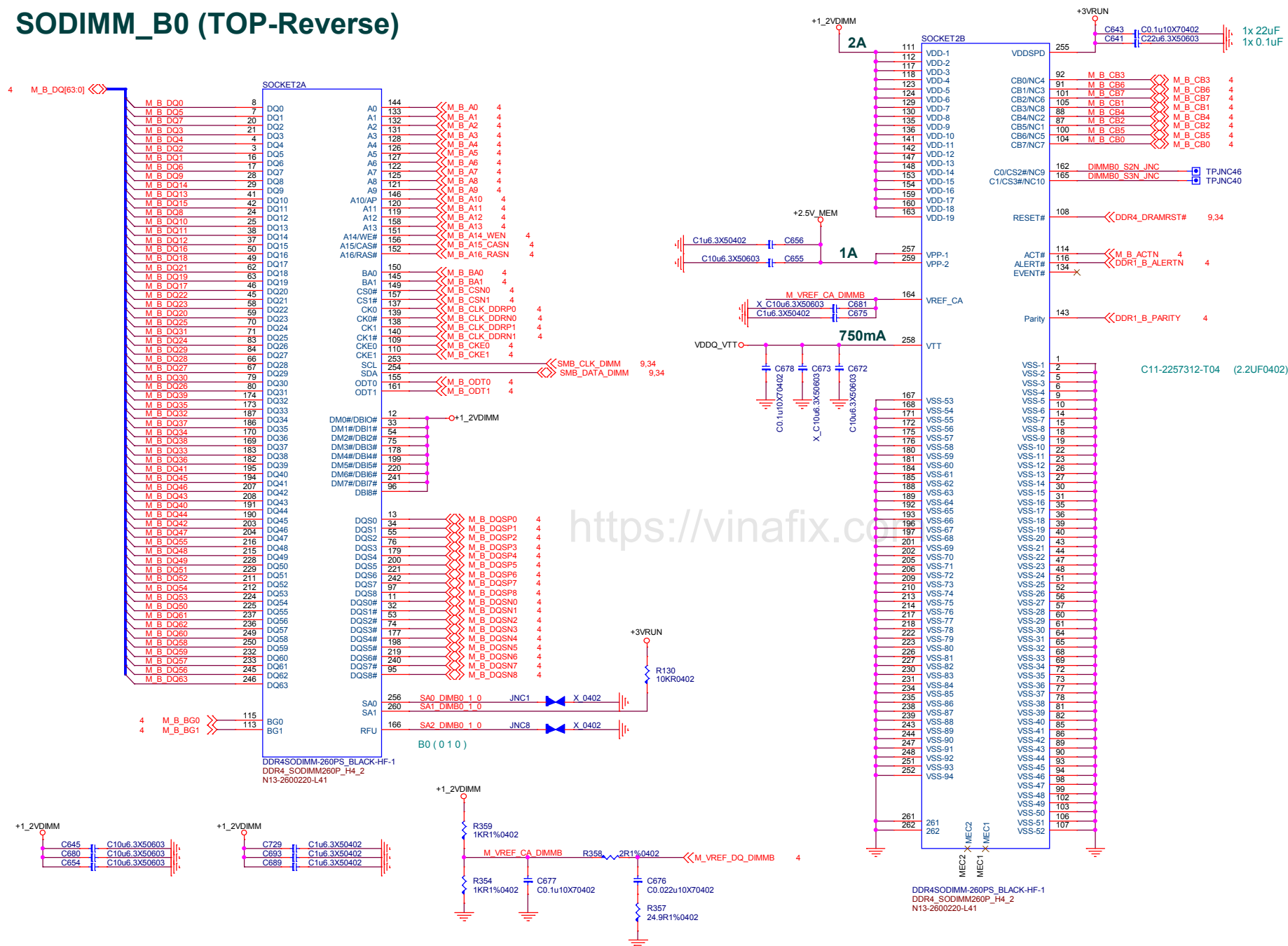




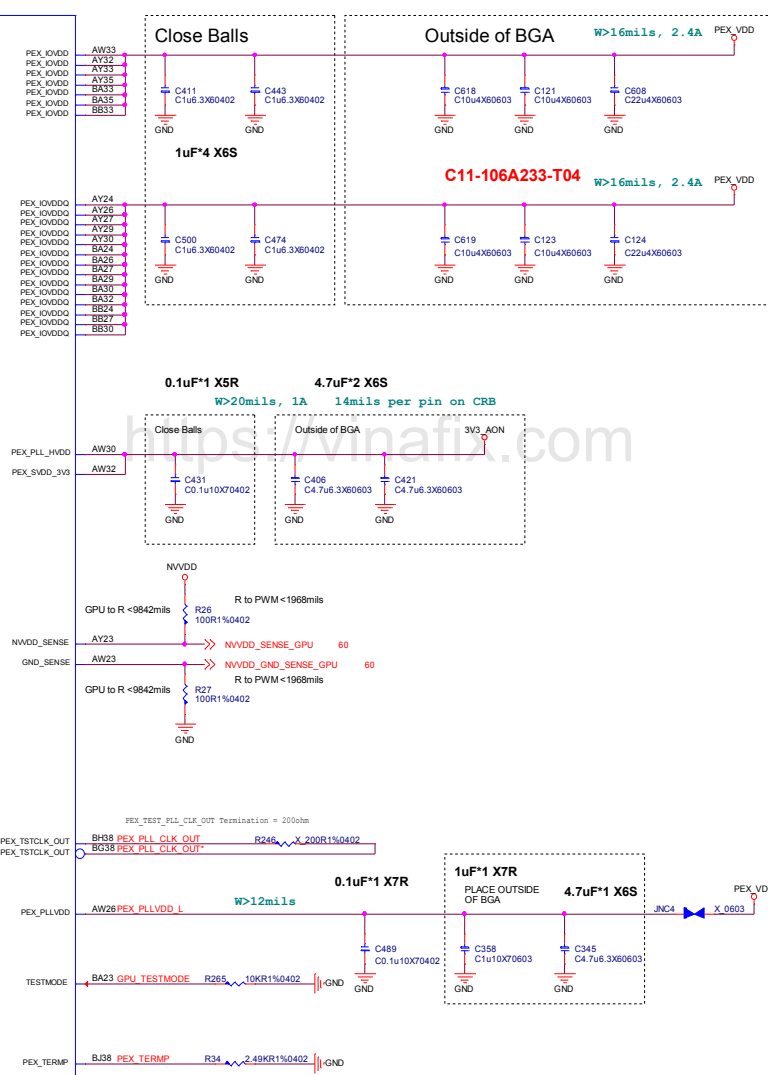
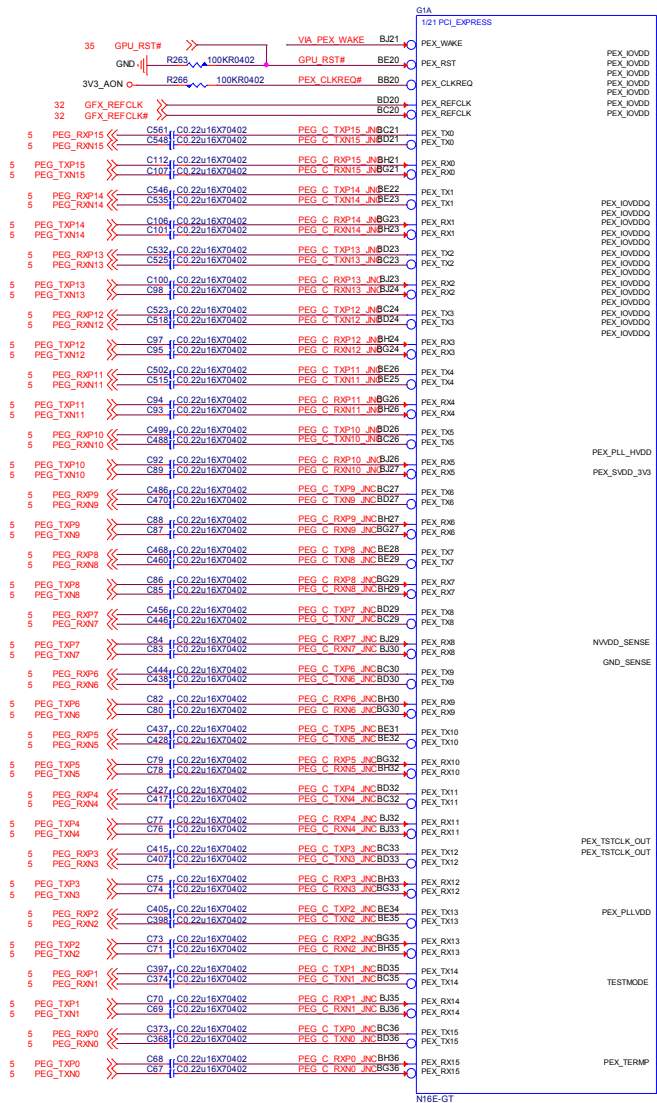
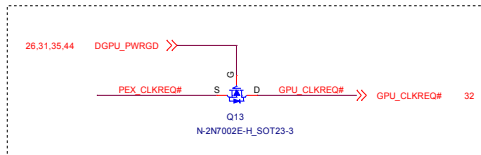
SODIMM_A0 (TOP-Standard)



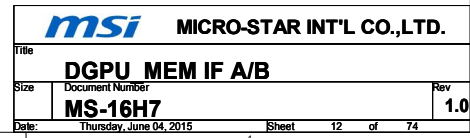
SODIMM_B0 (TOP-Reverse)



GPU PCI EXPRESS

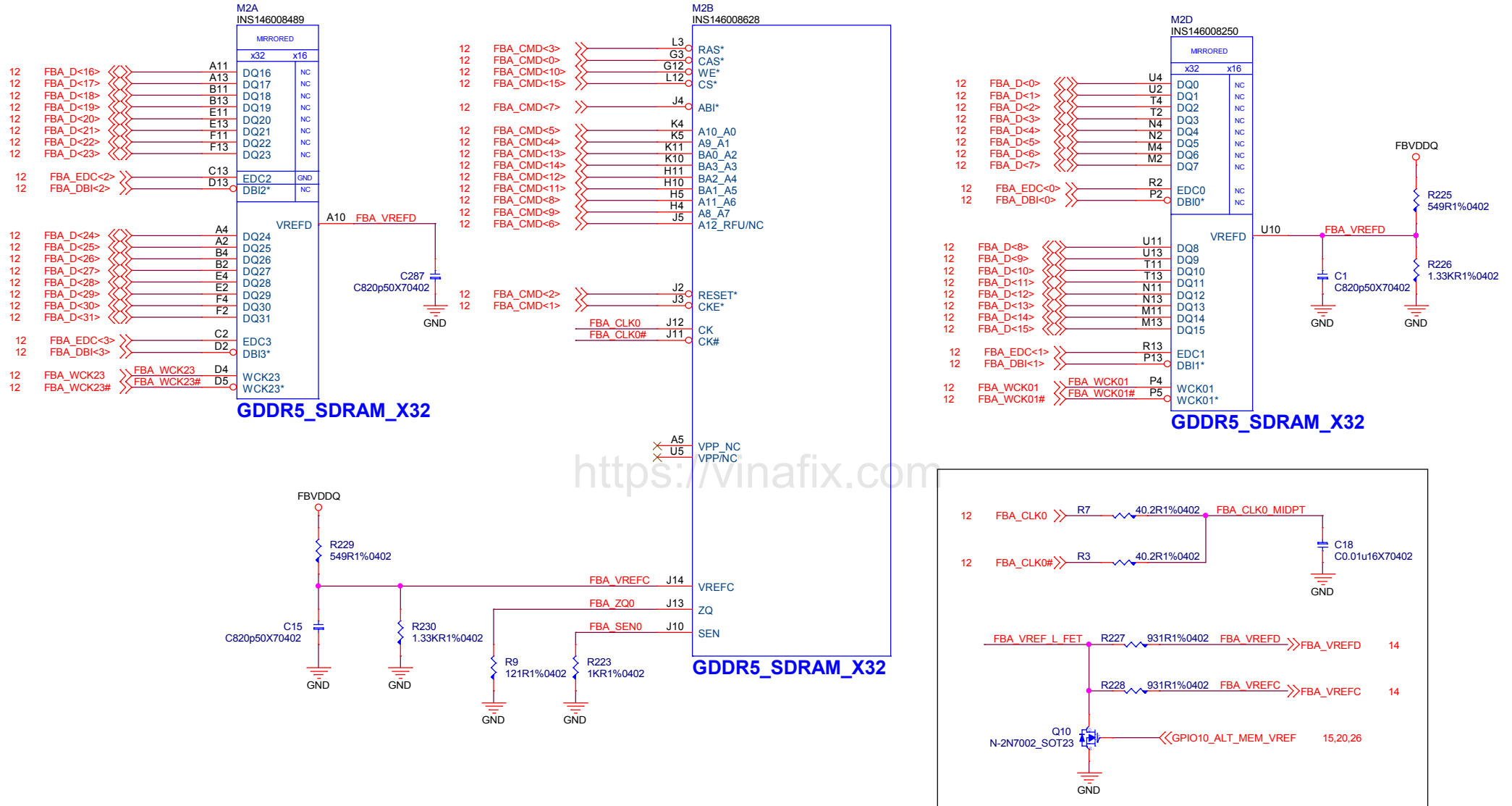


<https://vinafix.com>



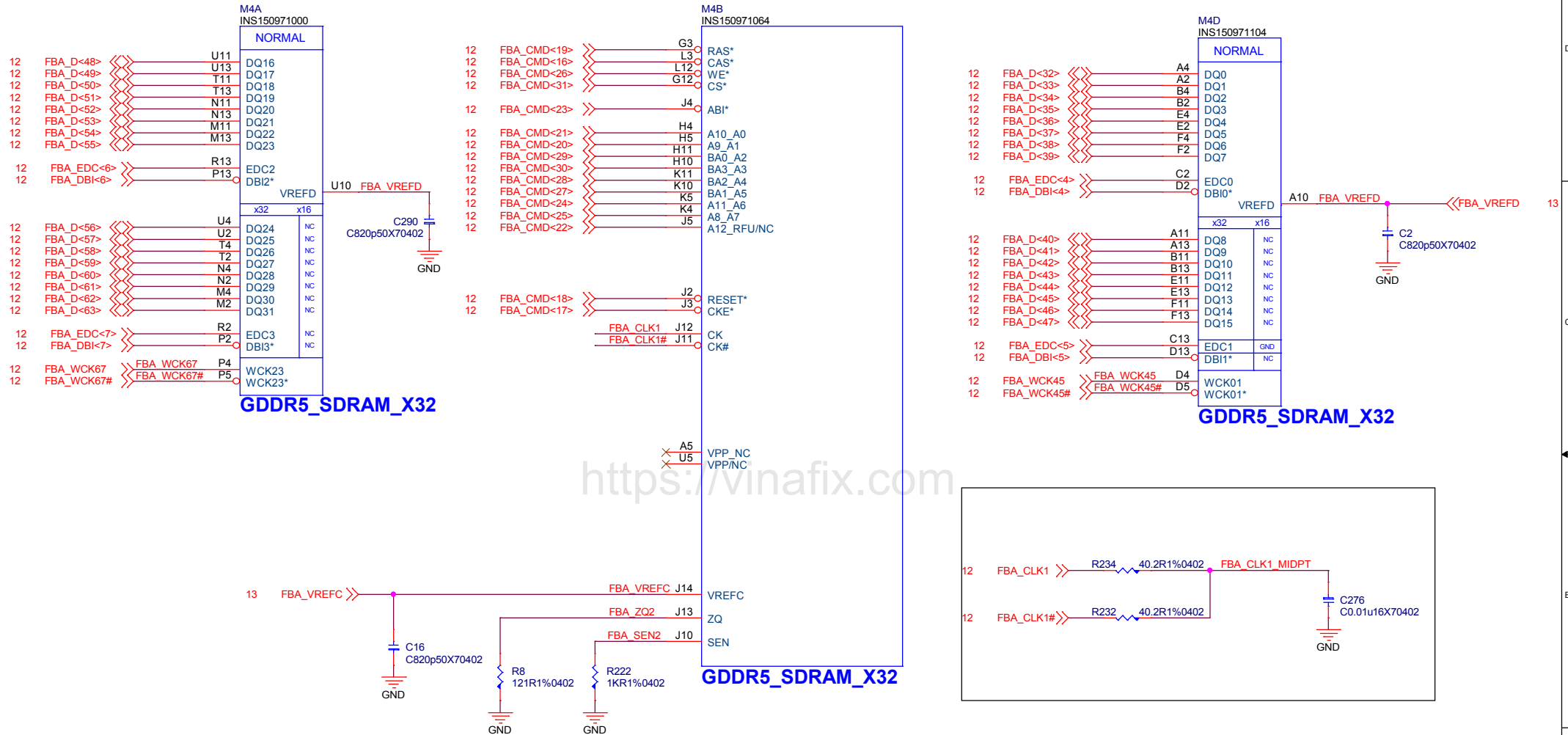
DGPU_GDDR5 FrameBuffer A0

M3 5010



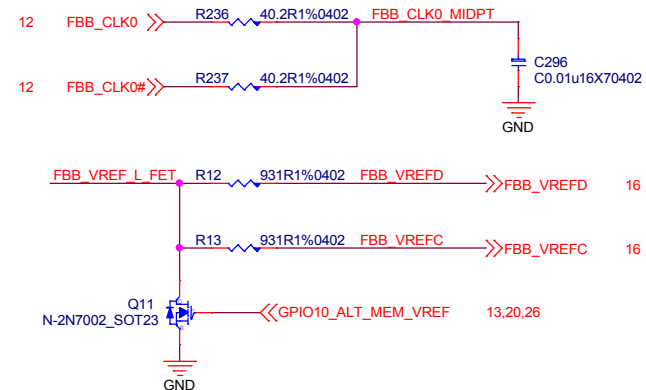
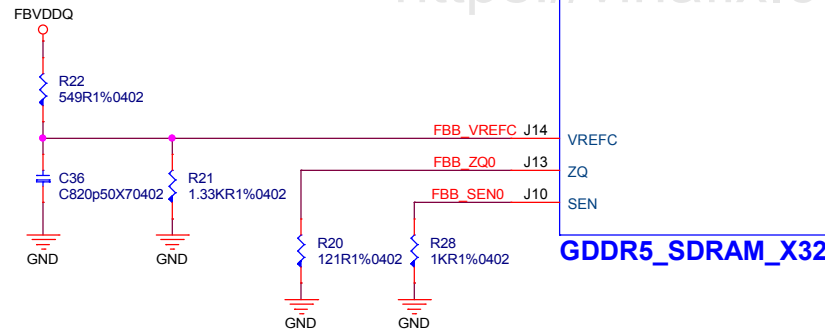
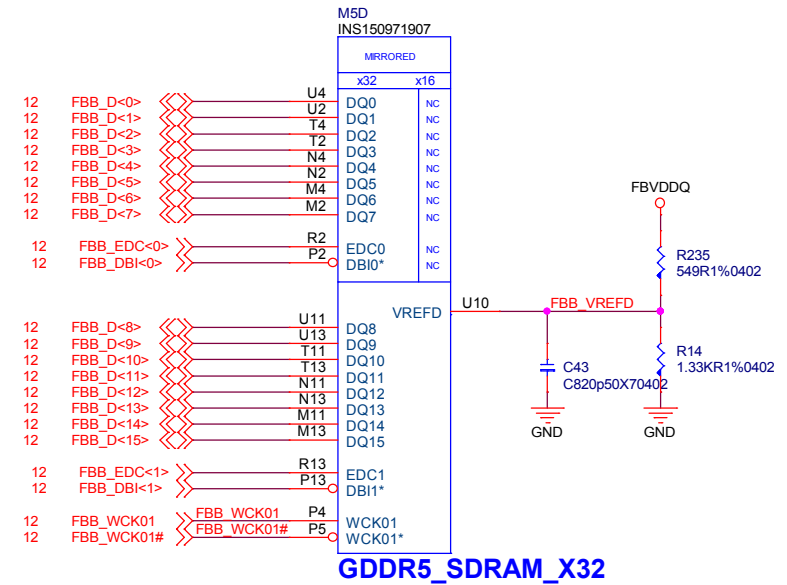
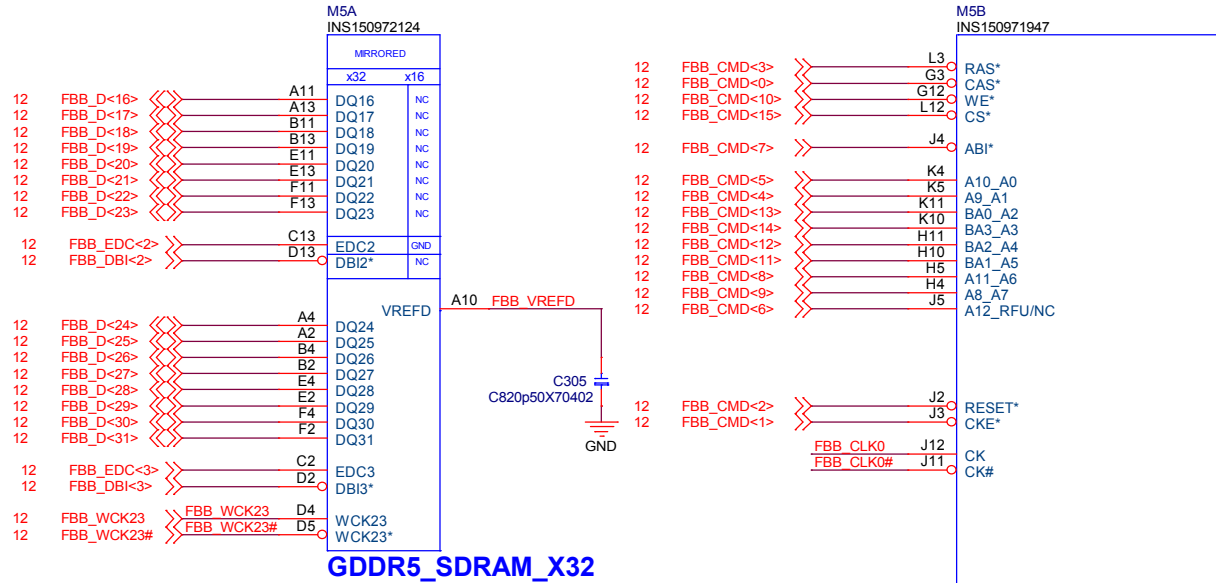
DGPU_GDDR5 FrameBuffer A1

M5 5010



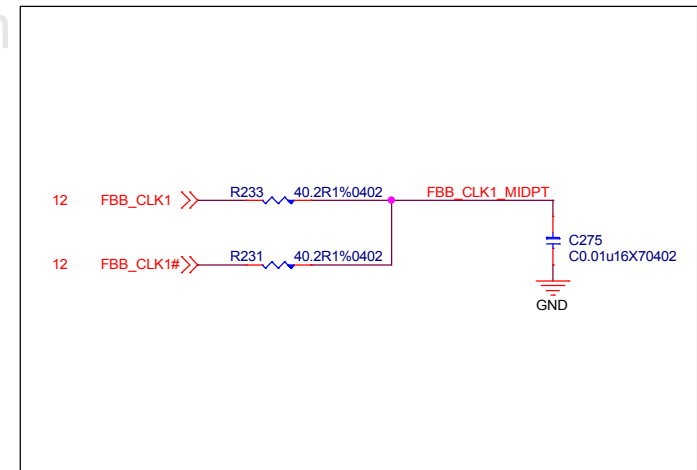
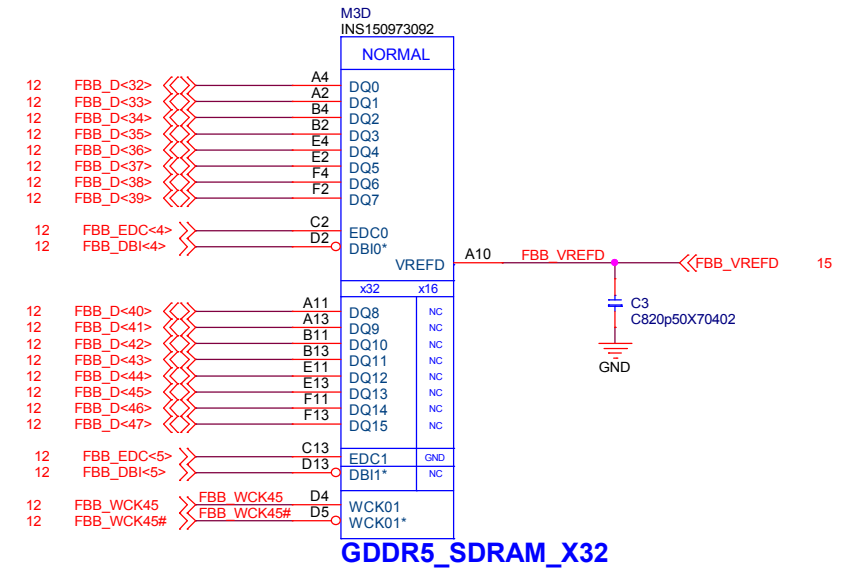
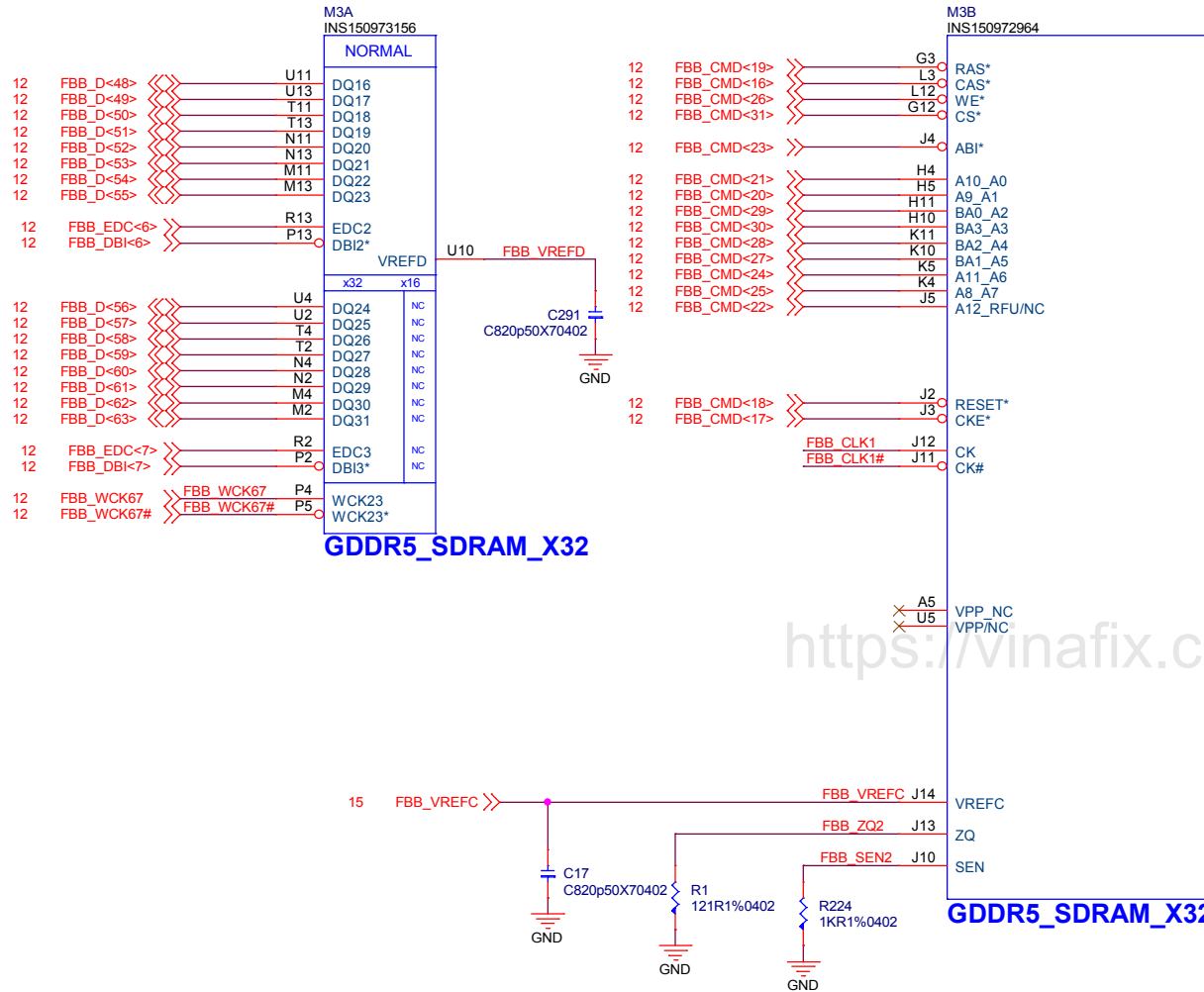
DGPU_GDDR5 FrameBuffer B0

M6 5010

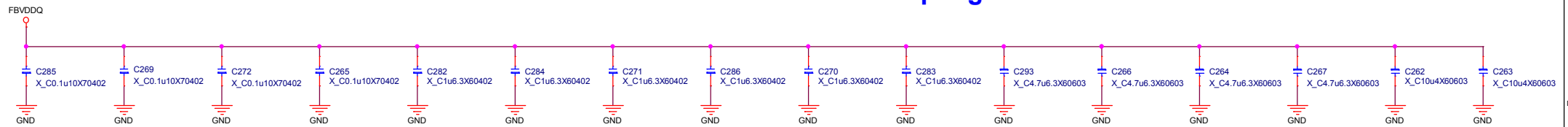


DGPU_GDDR5 FrameBuffer B1

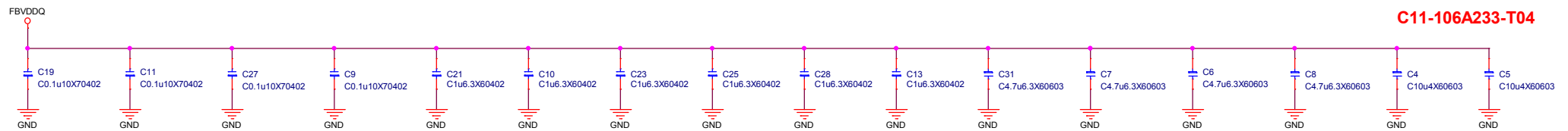
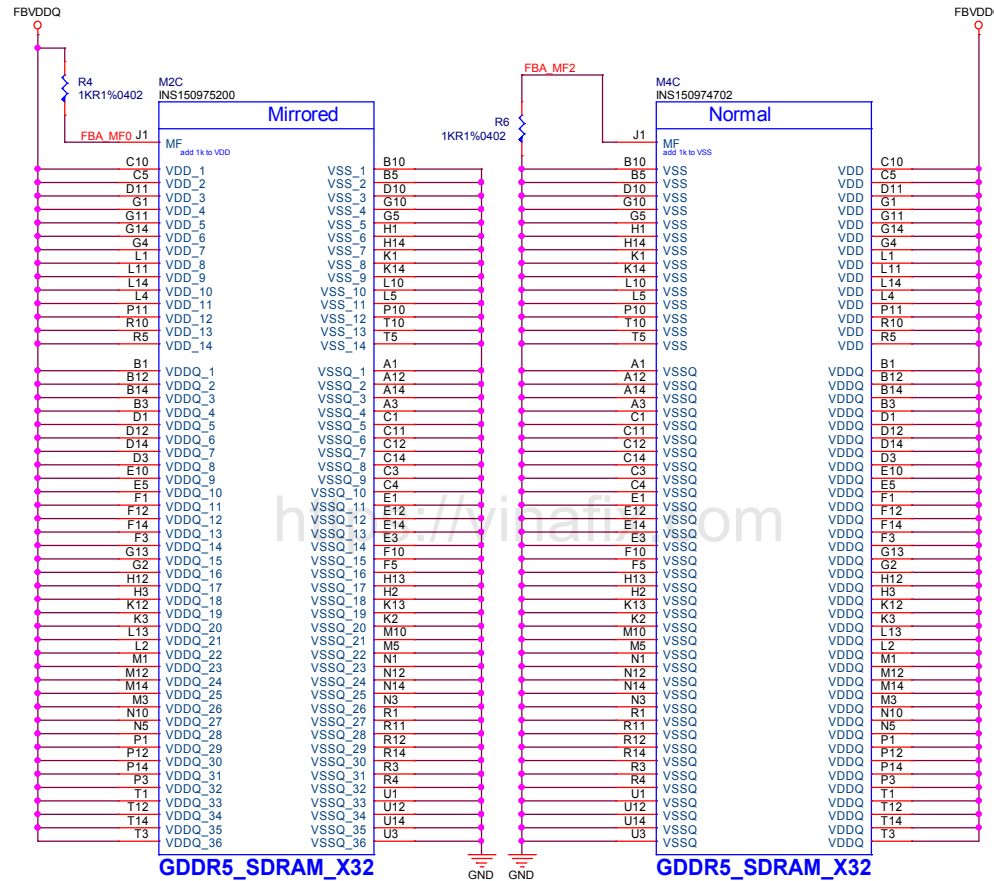
M4 5010



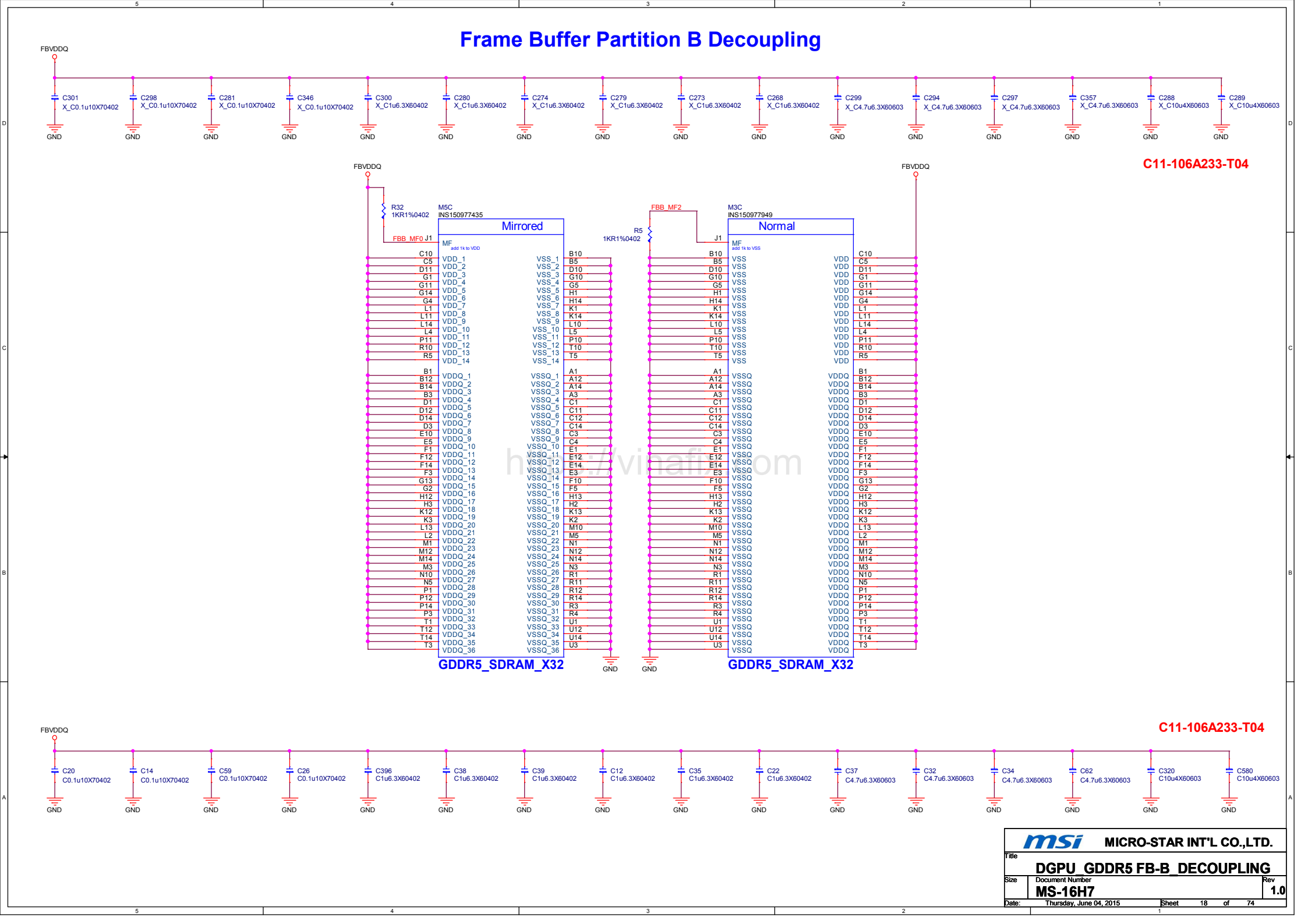
Frame Buffer Partition A Decoupling



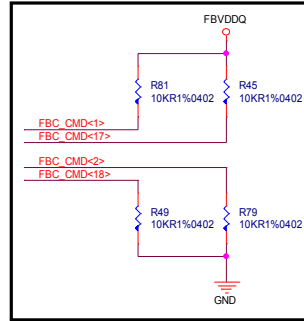
C11-106A233-T04



Frame Buffer Partition B Decoupling

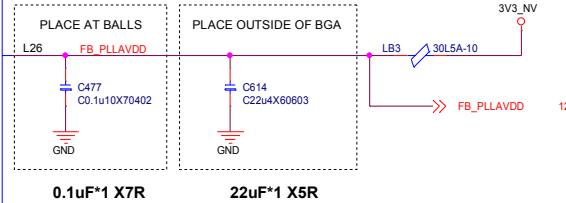
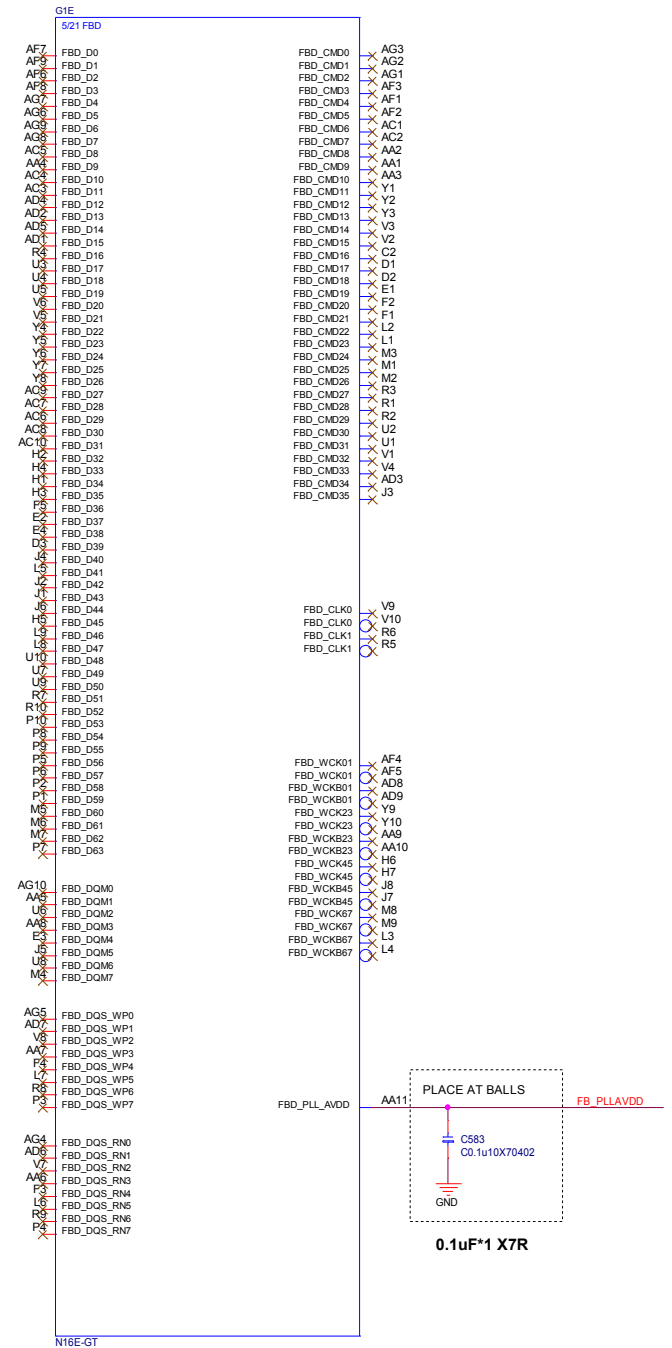


GPU Frame Buffer Partition C/D



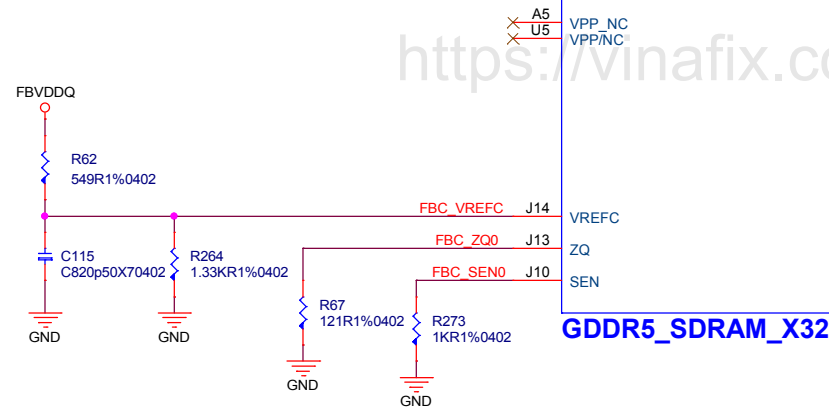
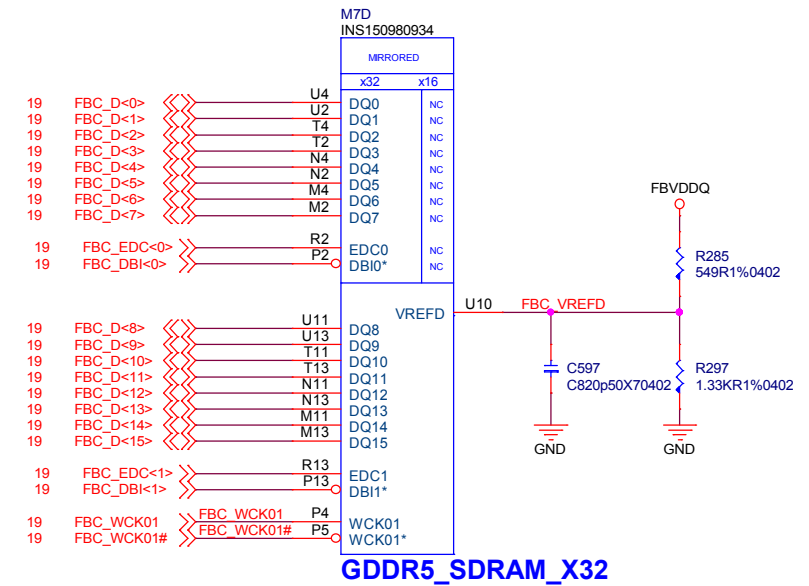
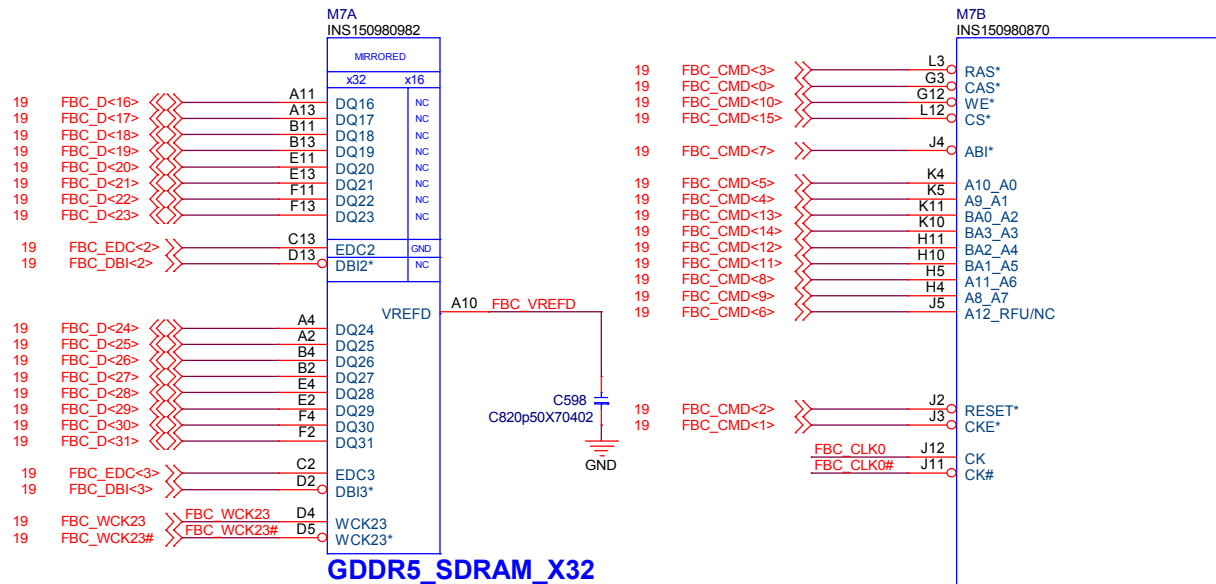
GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1 A9	
CMD5	A0 A10	
CMD6	A12 REFU	
CMD7	AB1*	
CMD8	A6 A11	
CMD9	A7 A8	
CMD10	WE*	
CMD11	A5 BA1	
CMD12	A4 BA2	
CMD13	A2 BA0	
CMD14	A3 BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1 A9
CMD21		A0 A10
CMD22		A12 REFU
CMD23		AB1*
CMD24		A6 A11
CMD25		A7 A8
CMD26		WE*
CMD27		A5 BA1
CMD28		A4 BA2
CMD29		A2 BA0
CMD30		A3 BA3
CMD31		CS*

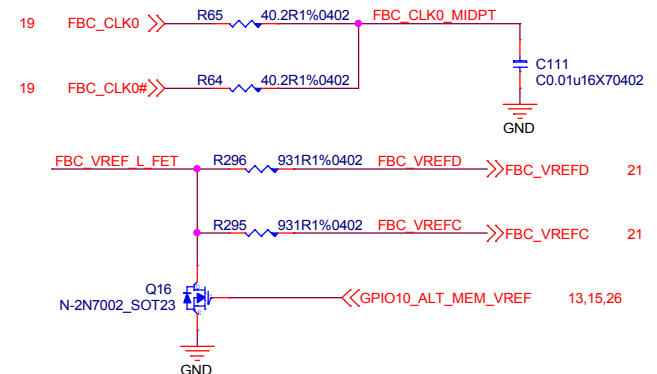


msi MICRO-STAR INT'L CO.,LTD.

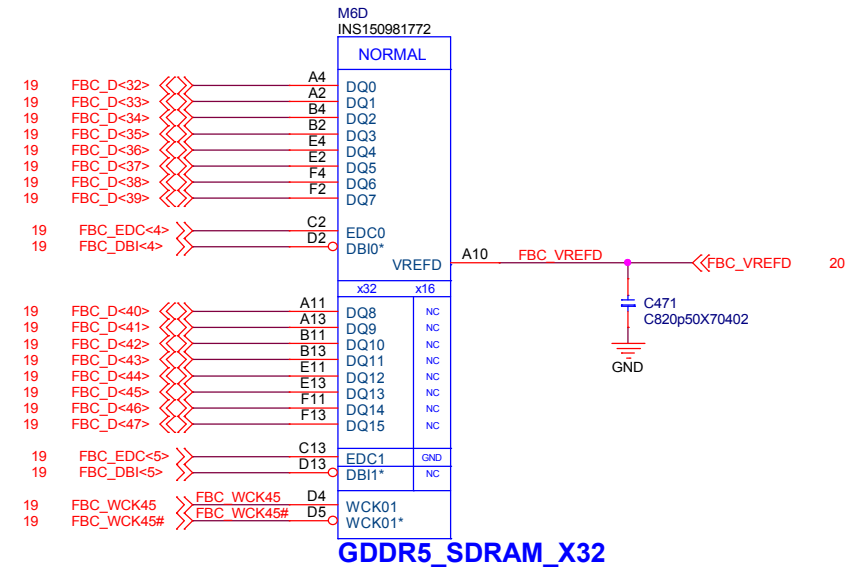
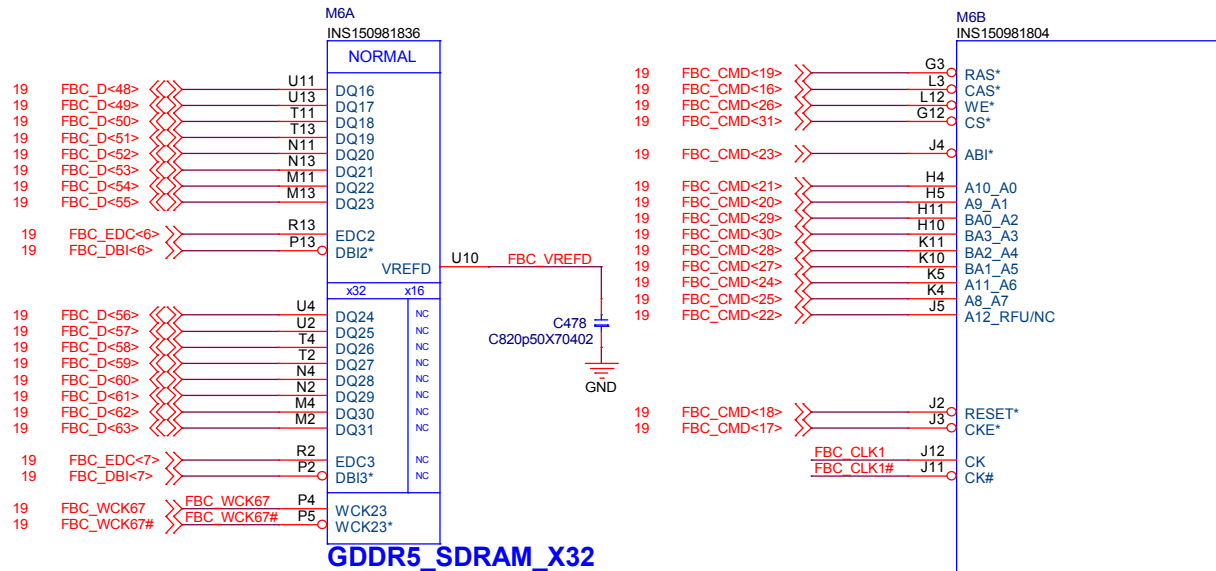
M9 5010



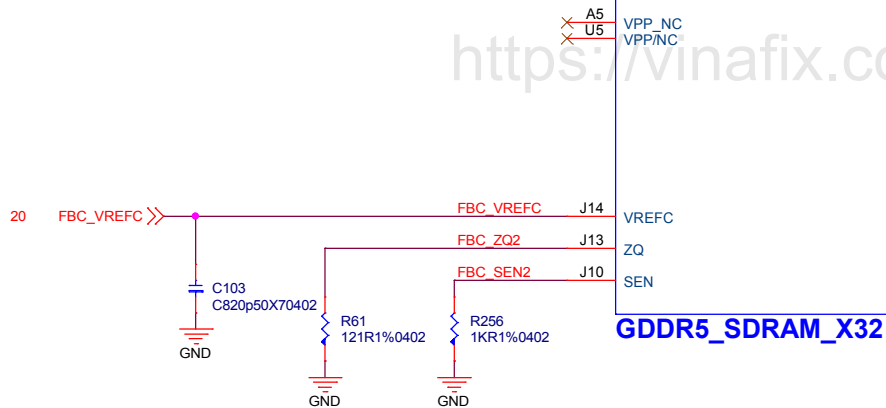
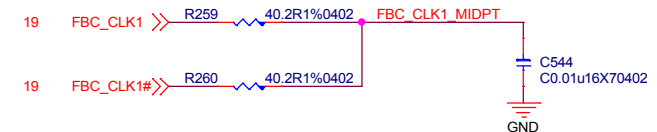
R227, R221, C501 unstuff when N15P-GX-B



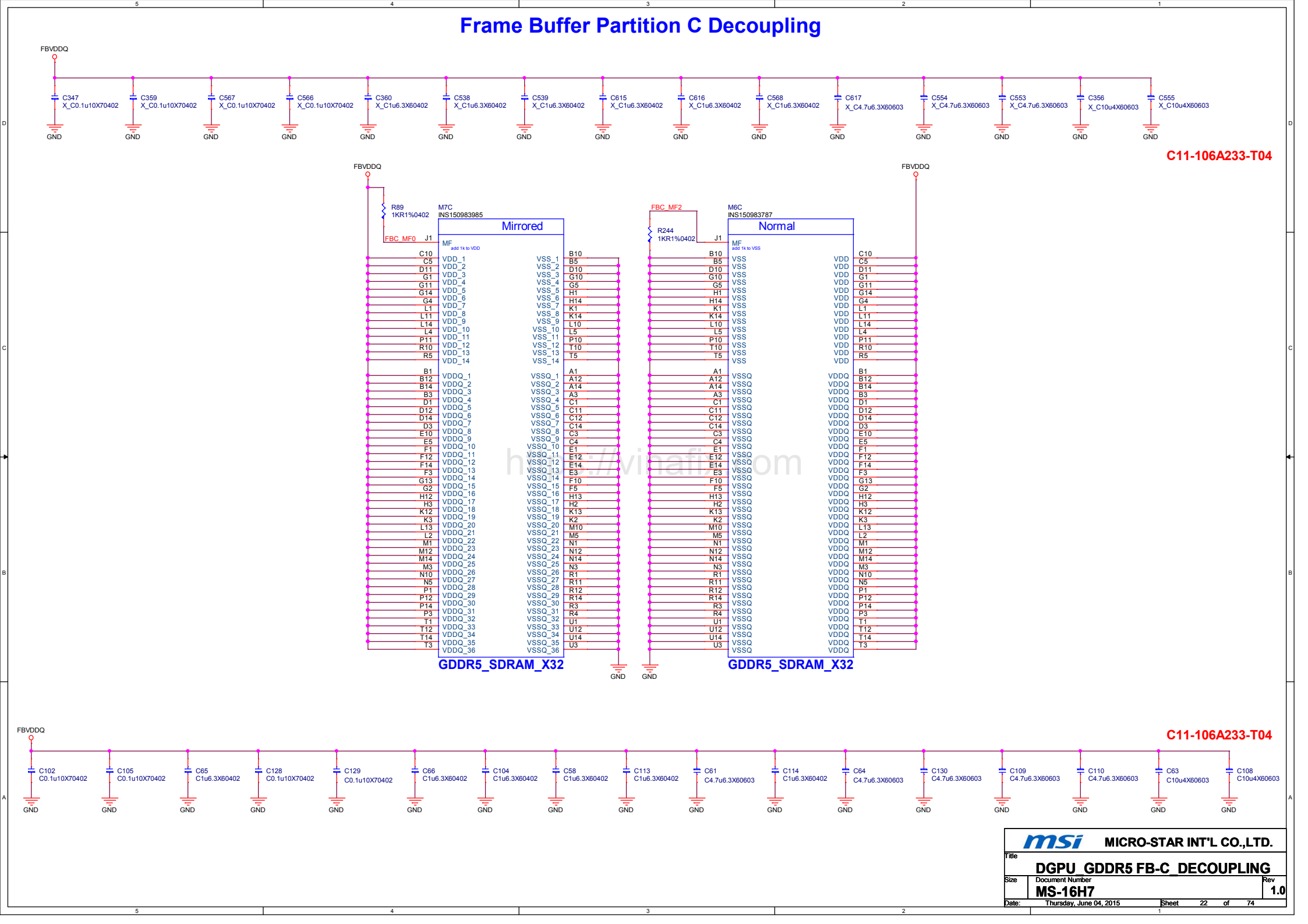
M8 5010



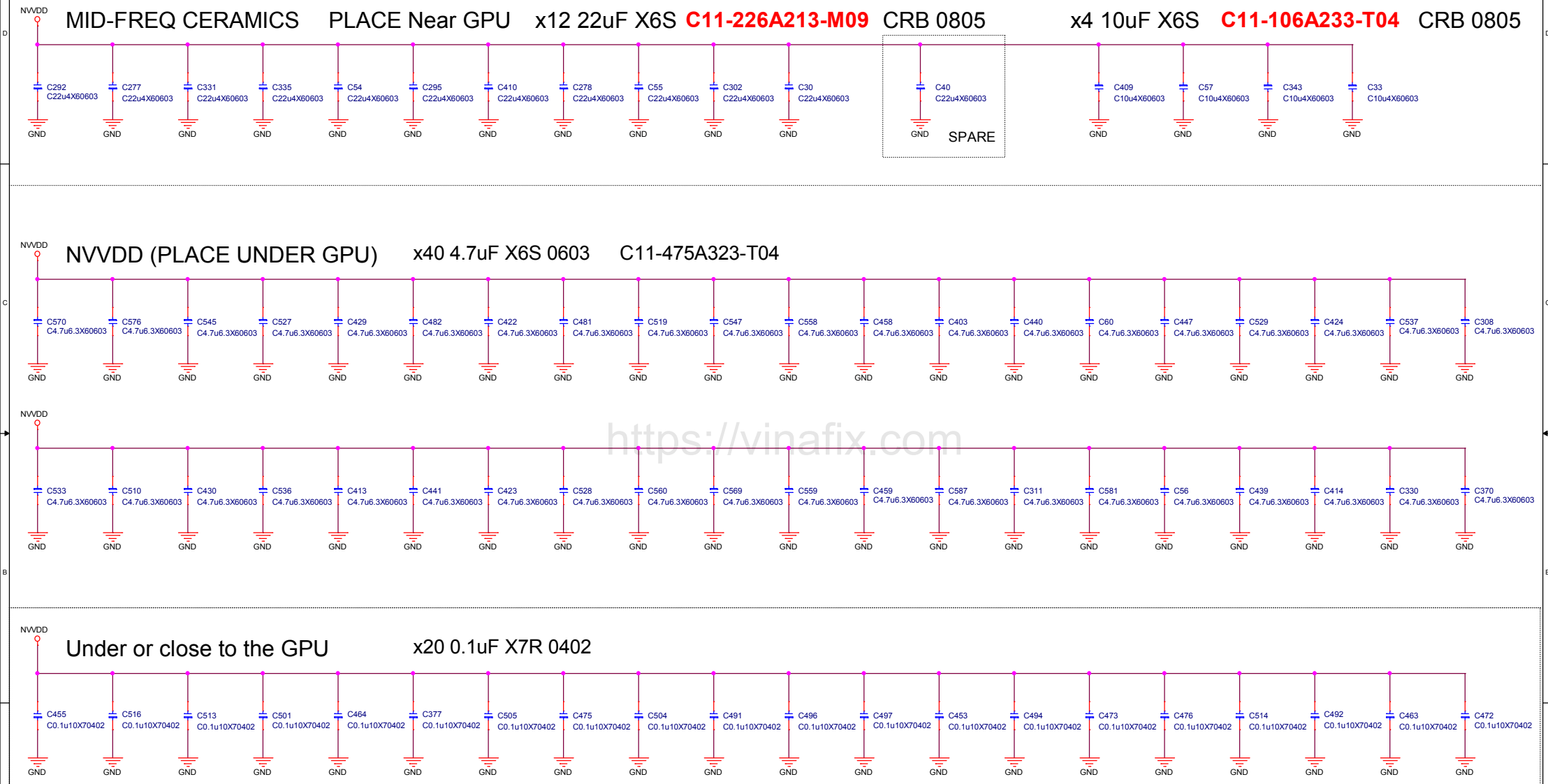
R227, R221, C501 unstuff when N15P-GX-B



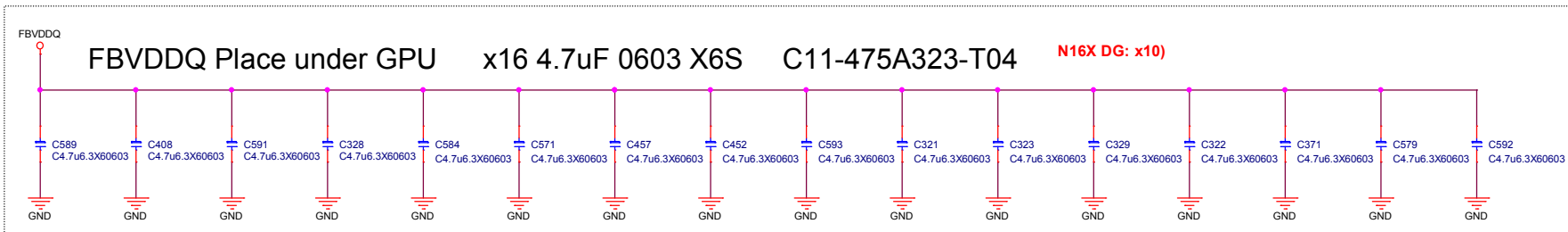
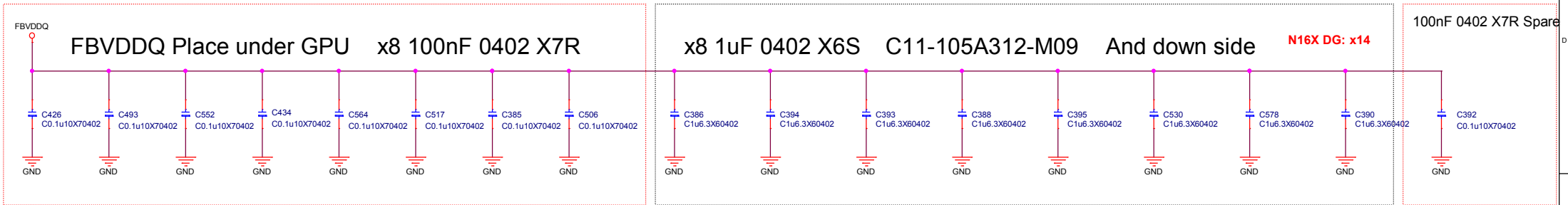
Frame Buffer Partition C Decoupling



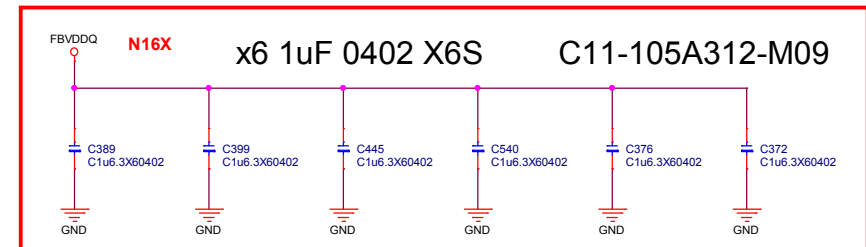
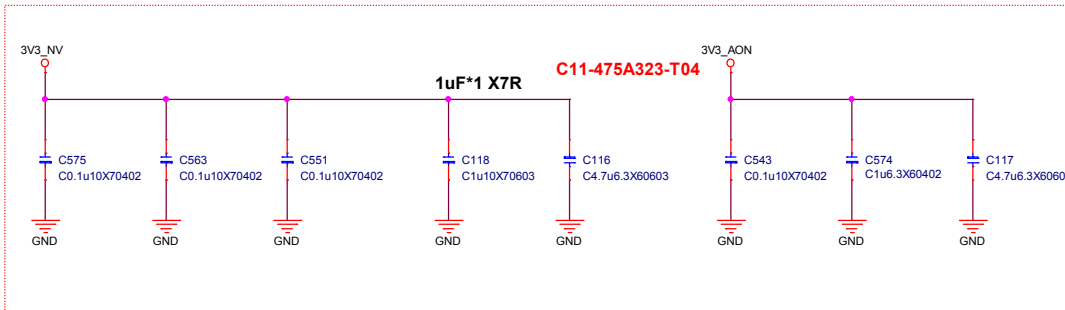
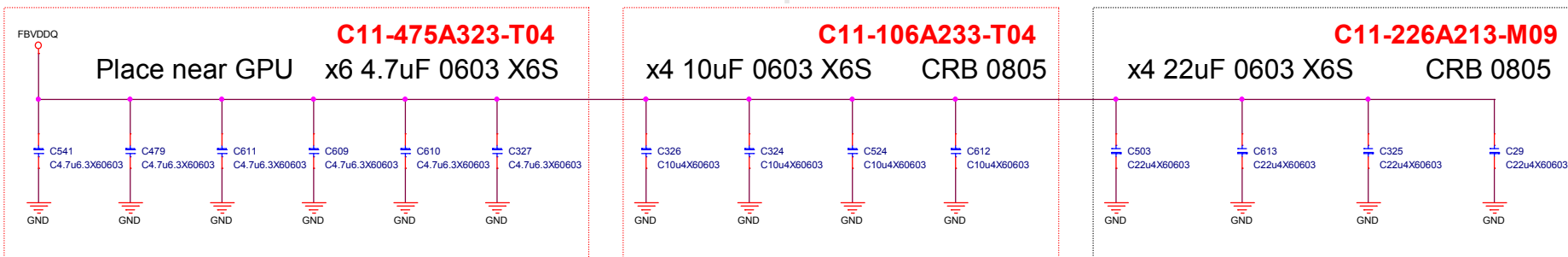
GPU DECOUPLING A



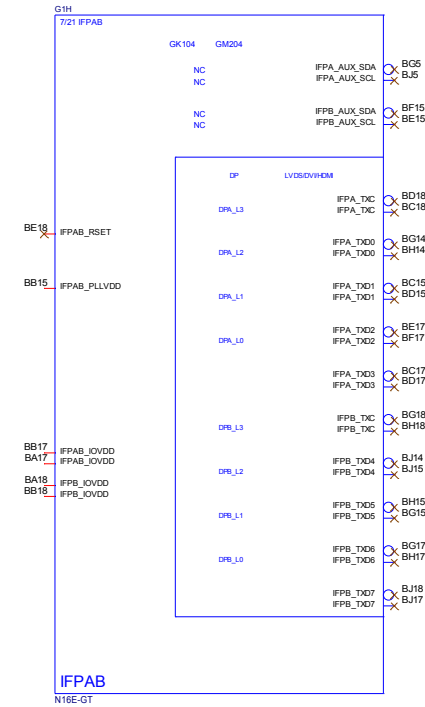
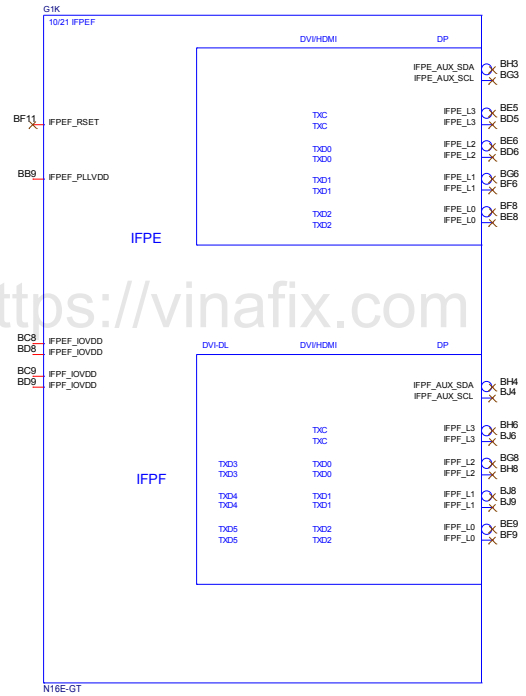
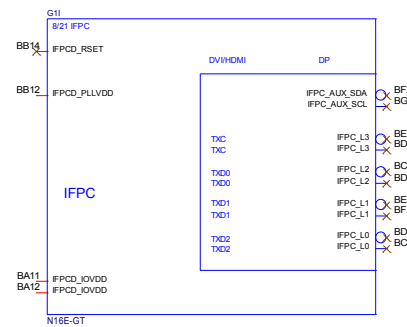
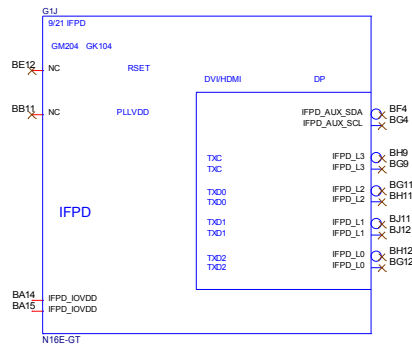
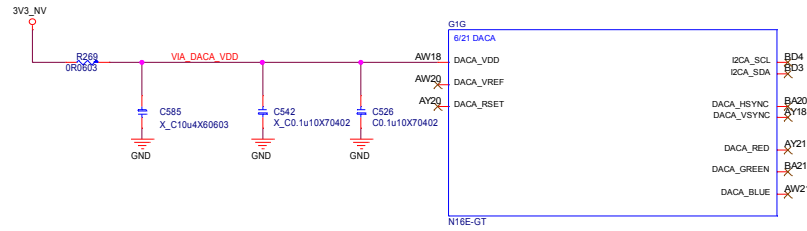
GPU DECOUPLING B



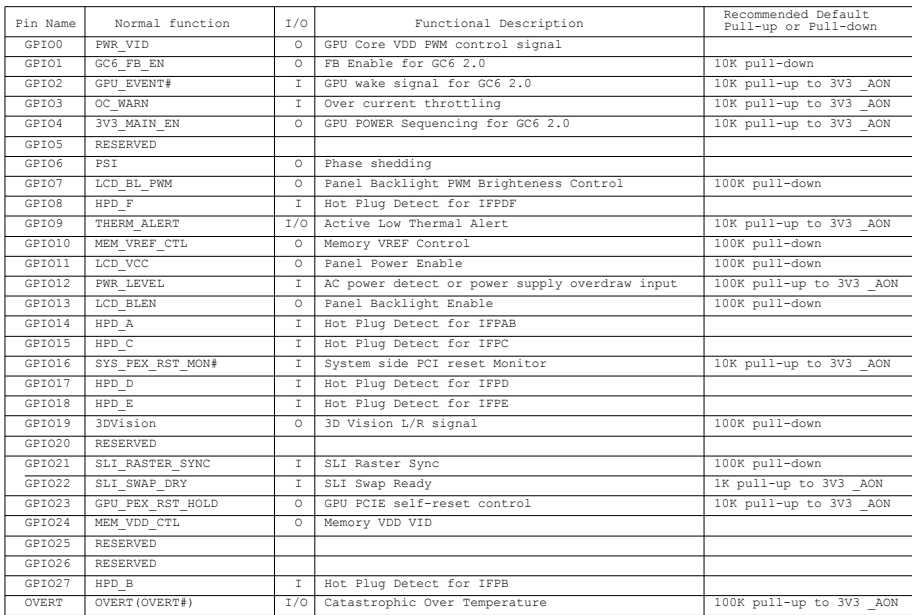
<https://vinafix.com>



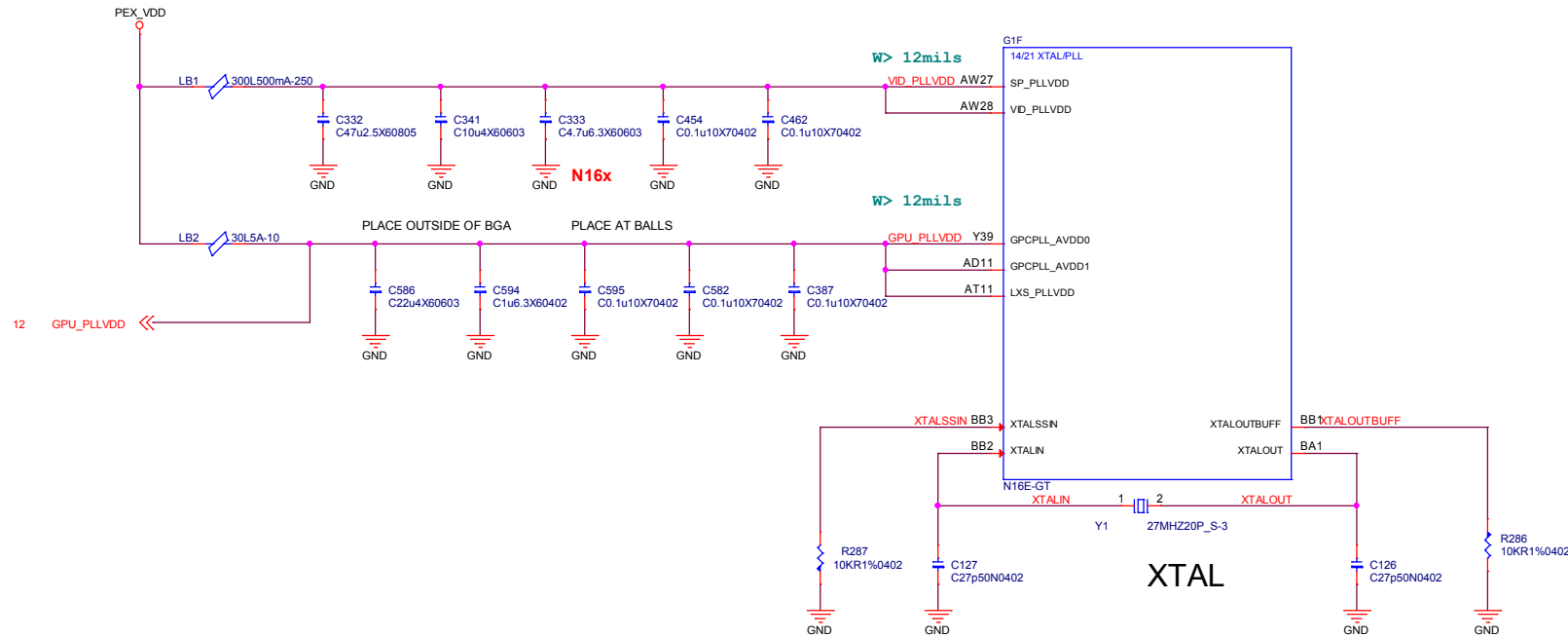
DACA, Display IF



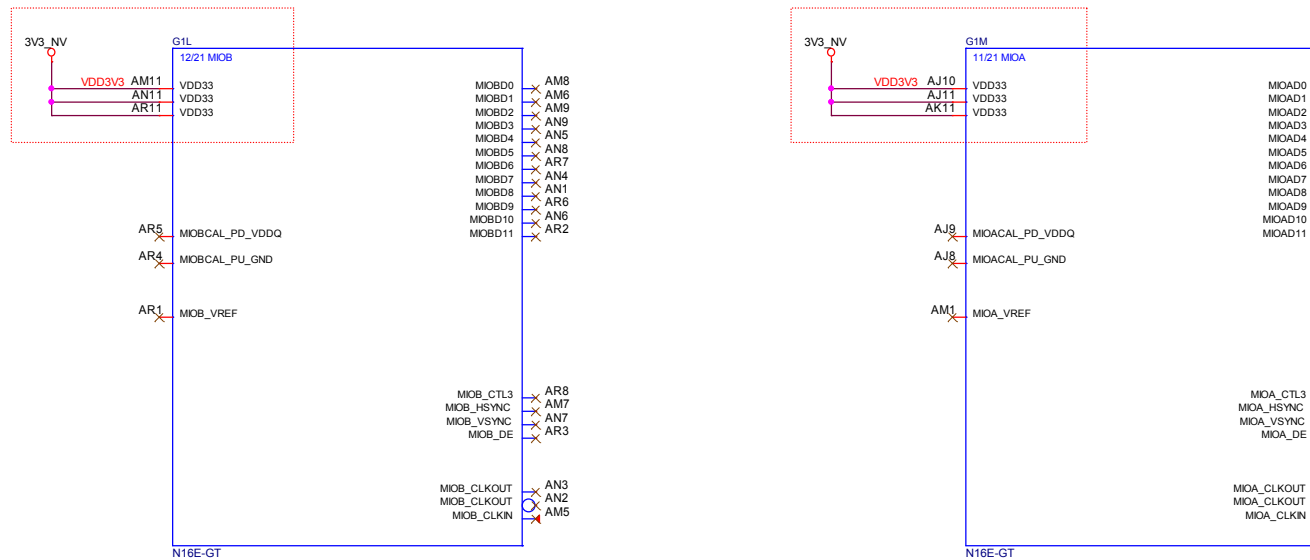
https://vinafix.com



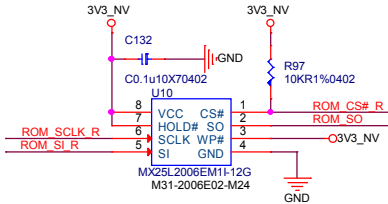
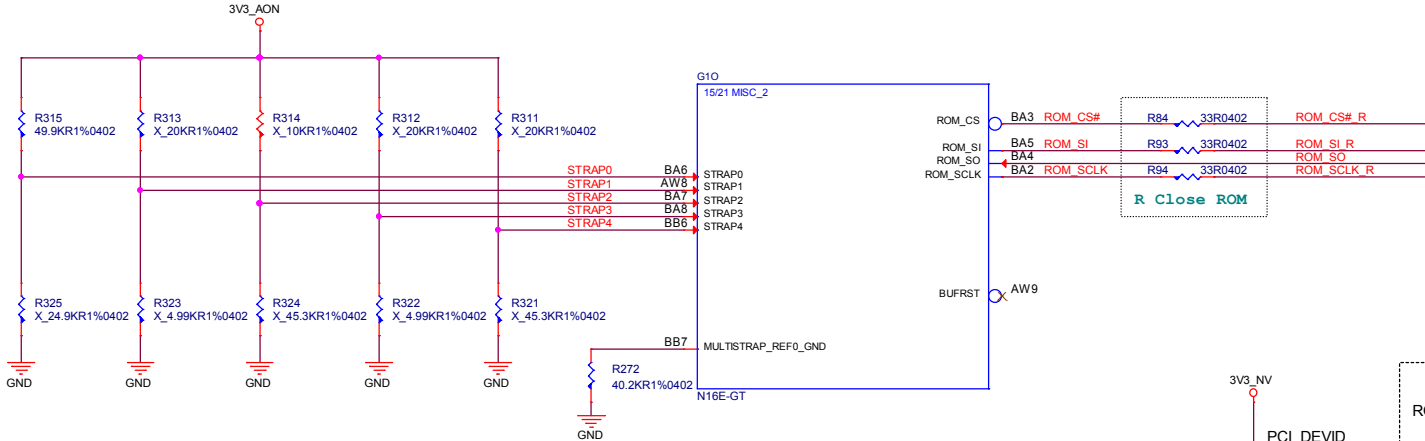
DGPU MIO & XTAL



Multi-use IO(MIO) Interface



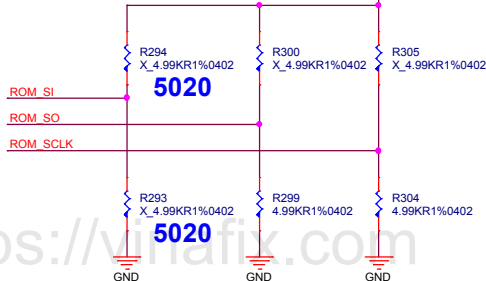
ROM, MULTI-LEVEL STRAPS



3G/2G

PU4K99 Hynix 256Mx32bit R11-4991T12-W08 X_4.99KR1%0402	V_TOP1 5010 M12-5GC4H65-H23 X_H5GC4H24AJR-T2C
PD20K Samsung 256Mx32bit R11-0203T12-W08 X_20KR1%0402	V_TOP2 5010 M12-4132525-S02 X_K4G41325FC-HC03
PD24R9 Micron 256Mx32bit R11-249AT12-W08 X_24.9R1%0402	V_TOP3 5010 M12-4032B05-E59 X_EDW4032BABG-60-F

GDDR5 Parts
5010 : M2 , M3 , M4 , M5 , M6 , M7



N16E_GS
B03-N16EG05-N08
N16E-GS-KCD-A1

N16E_GT
B03-0N16E25-N08
N16E-GT-A1

	N16E-GS 2G		N16E-GT 3G	
ROM_SI	4K99 PU	Hynix 256x32bit	4K99 PU	Hynix 256x32bit
	20K PD	Samsung 256x32bit	20K PD	Samsung 256x32bit
	24R9 PD	Micron 256x32bit	24R9 PD	Micron 256x32bit
ROM_SO	5K PD		5K PD	
ROM_SCLK	5K PD		5K PD	
STRAP0	50K PU 3V3_AON		50K PU 3V3_AON	
STRAP1	Reserved		Reserved	
STRAP2	Reserved		Reserved	
STRAP3	Reserved		Reserved	
STRAP4	Reserved		Reserved	

msi MICRO-STAR INT'L CO.,LTD.

Title: **DGPU ROM,HW Straps**

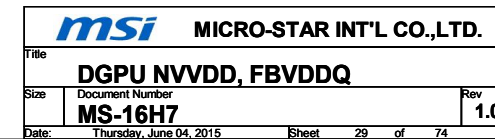
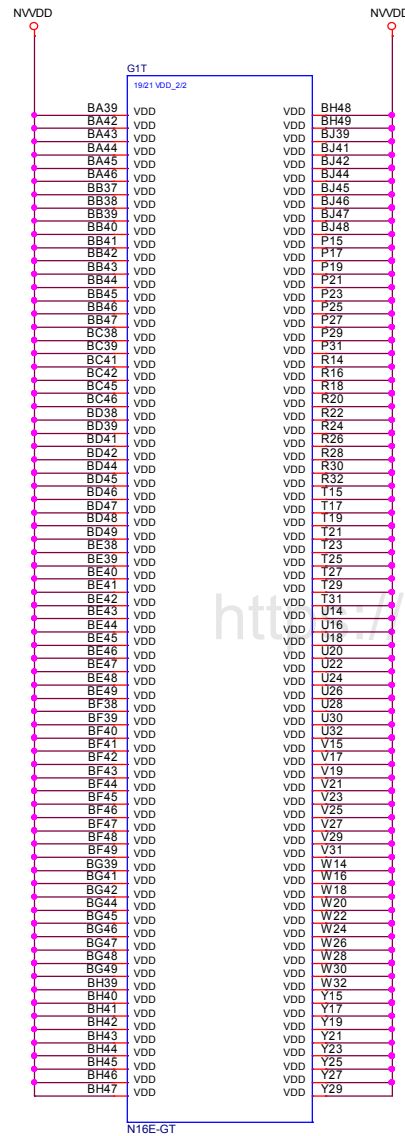
Size: **MS-16H7**

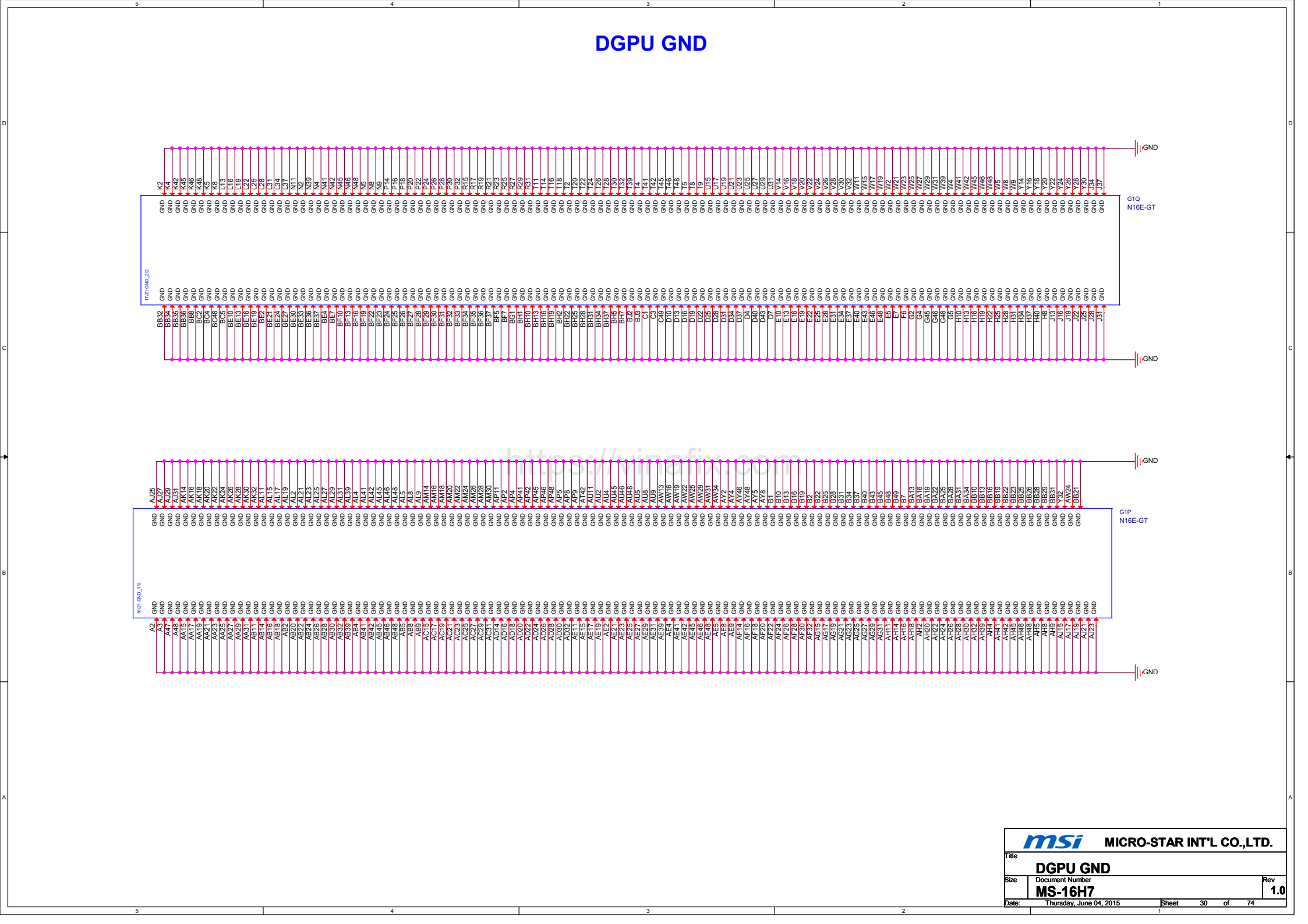
Date: Thursday, June 04, 2015

Sheet 28 of 74

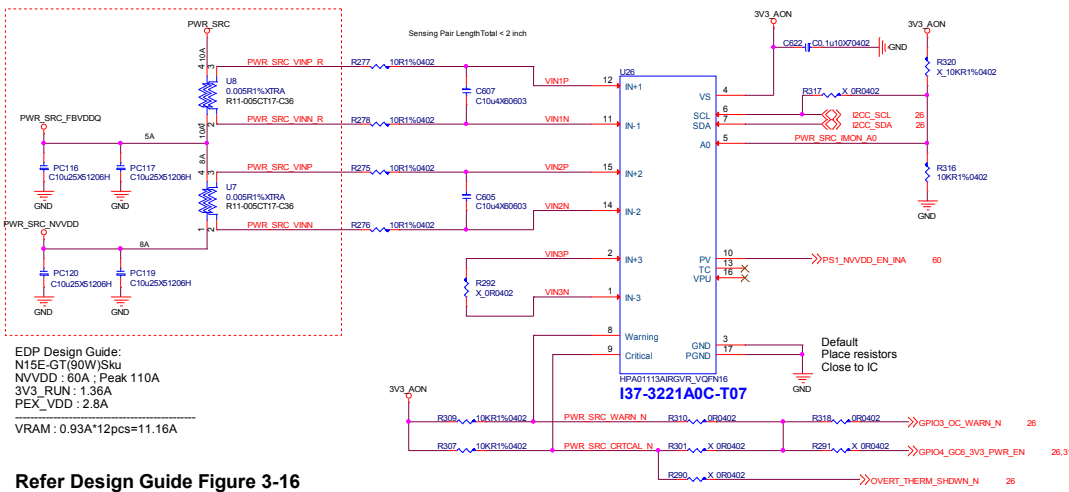
Rev 1.0

VDD T29
VDD T31
VDD U14
VDD U16
VDD U18

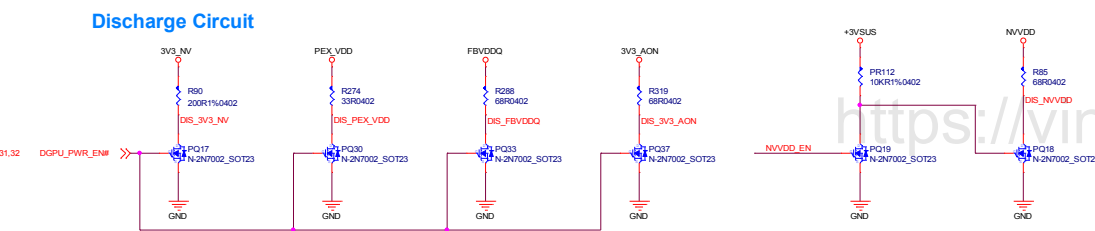


[illegible]

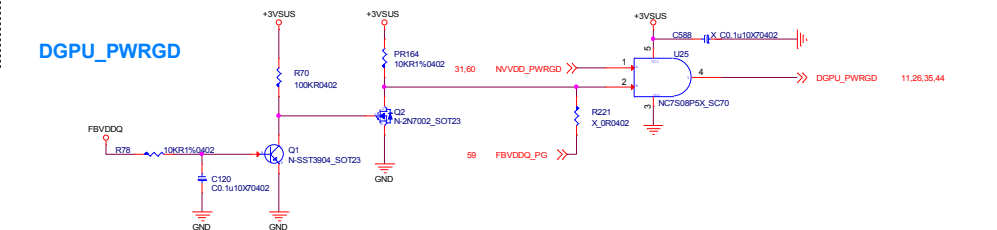
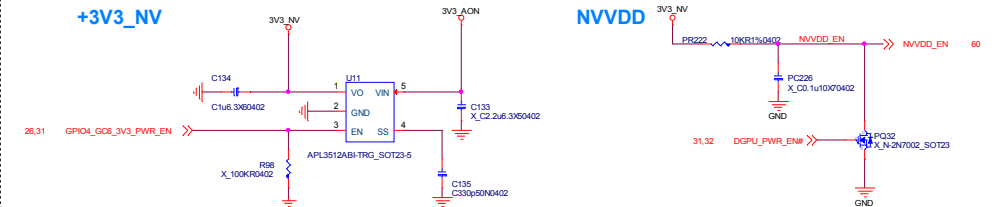
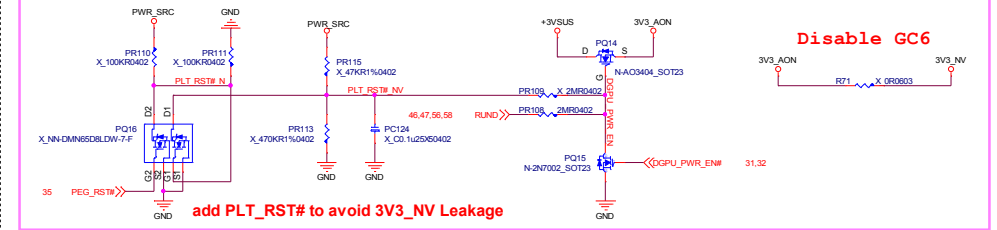
DGPU_Power Control



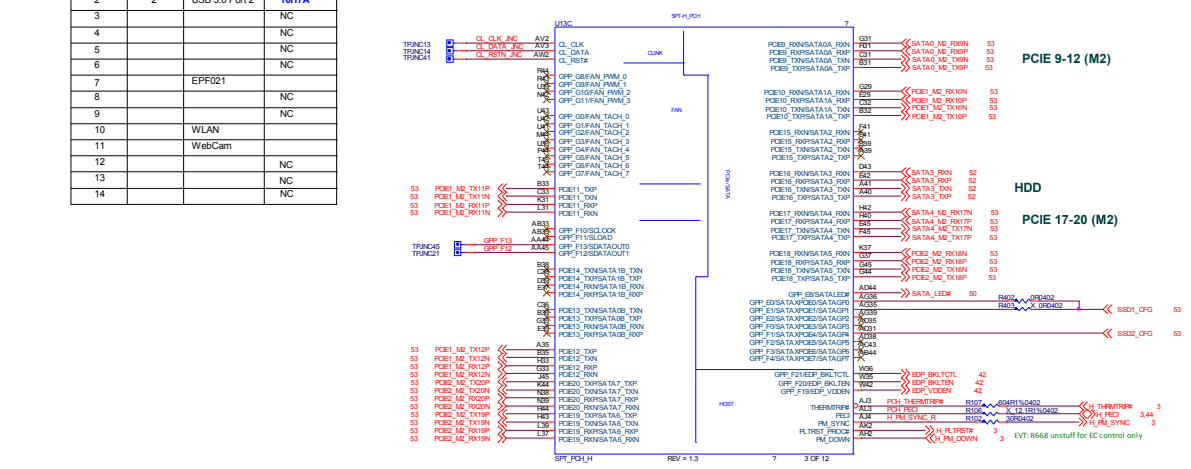
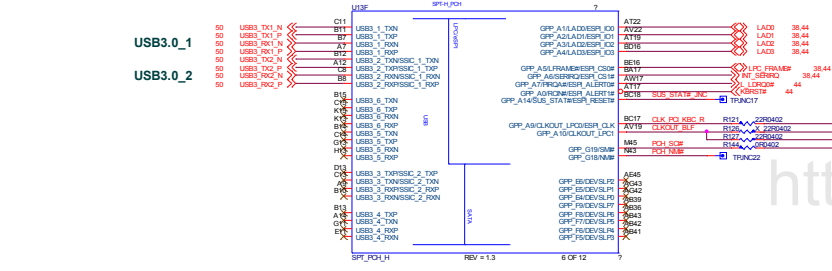
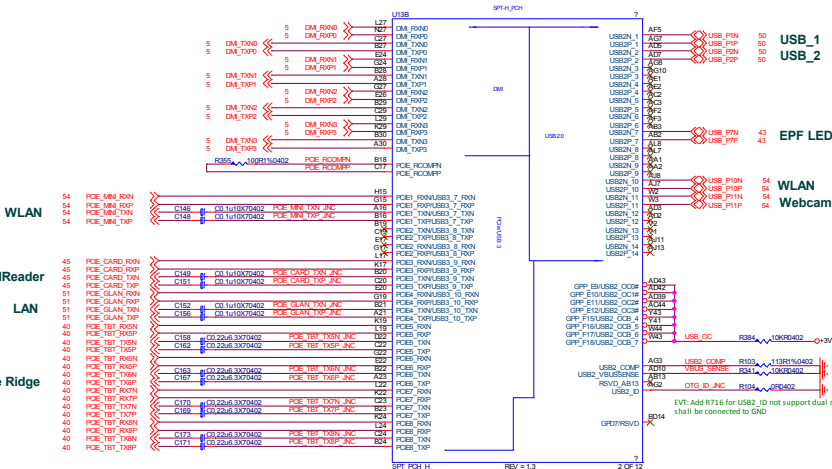
Refer Design Guide Figure 3-16



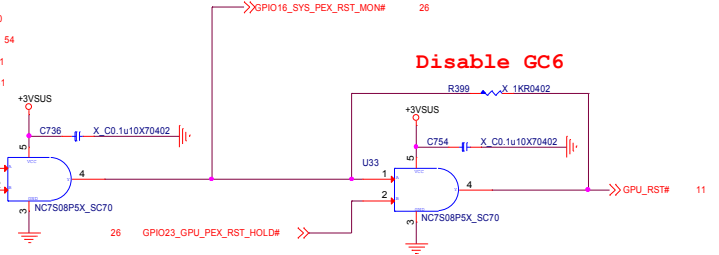
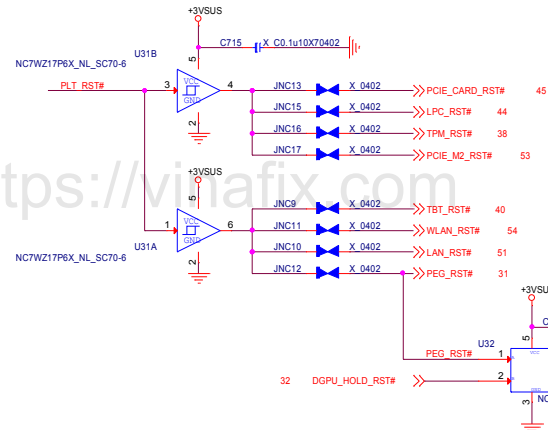
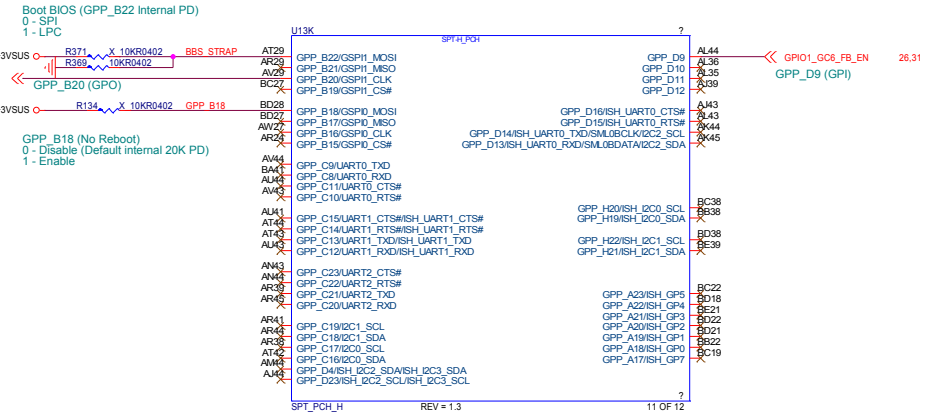
nVIDIA Power Sequence Control 3V3_NV -> NVVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD



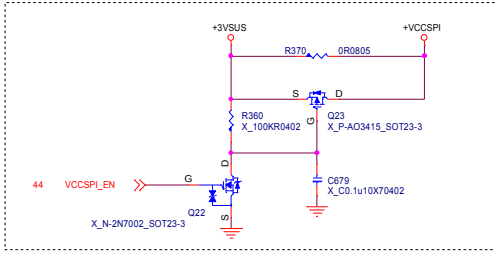
USB			
USB 2.0	USB 3.0	Device	Note
1	1	USB 3.0 Port 1	16H7A
2	2	USB 3.0 Port 2	16H7A
3			NC
4			NC
5			NC
6			NC
7		EPF021	
8			NC
9			NC
10		WLAN	
11		WebCam	
12			NC
13			NC
14			NC

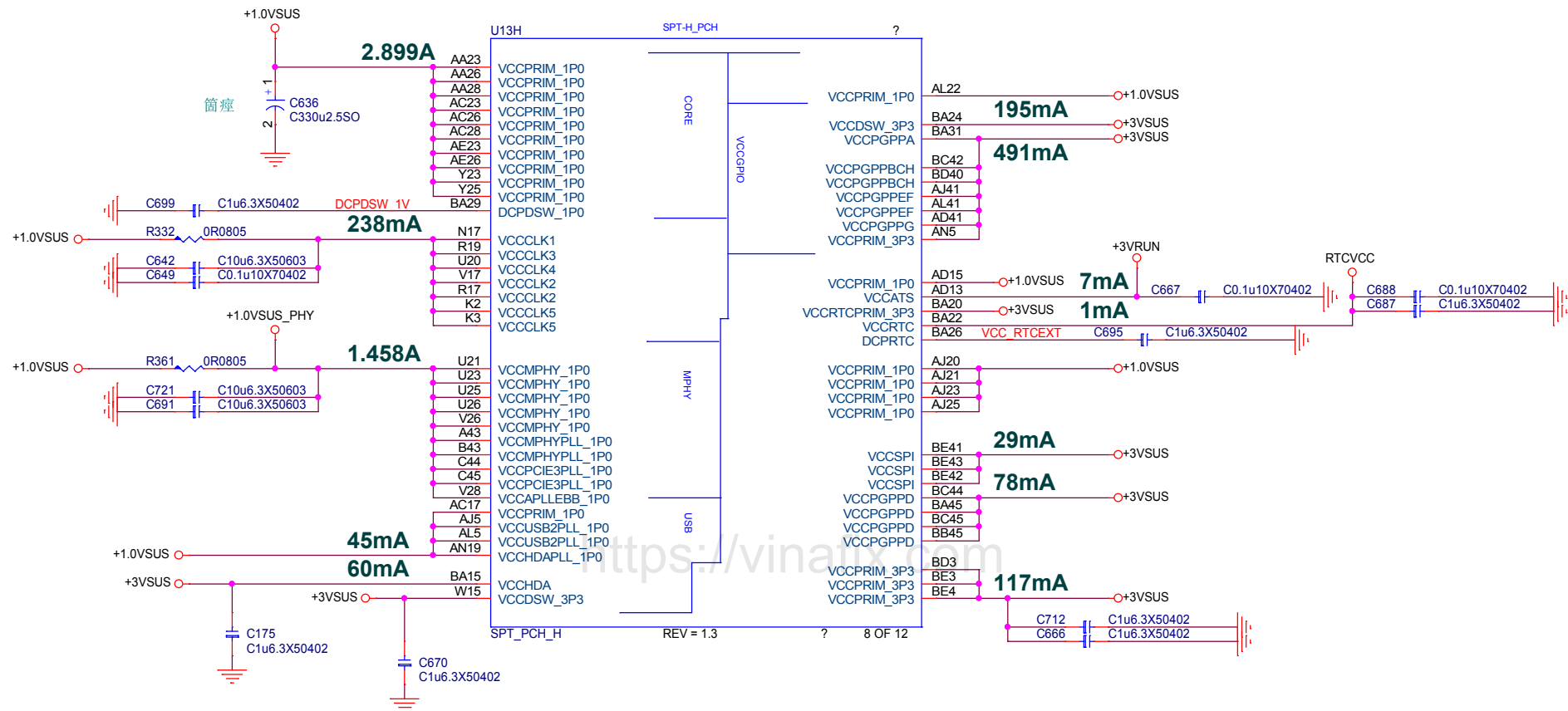



High Speed I/O Ports			
	HM170	C236	Device
1	USB3.0PCIE	USB3.0PCIE	WLAN
2	USB3.0PCIE	USB3.0PCIE	NC
3	PCIE	USB3.0PCIE	CardReader
4	PCIE	USB3.0PCIE	LAN
5	PCIE	PCIE	Alpine Ridge
6	PCIE	PCIE	
7	PCIE	PCIE	
8	PCIE	PCIE	
9	SATAPCIE	SATAPCIE	M2 SSD 1
10	SATAPCIE	SATAPCIE	
11	PCIE	PCIE	
12	PCIE	PCIE	
13	PCIE	SATAPCIE	NC
14	PCIE	SATAPCIE	NC
15	SATAPCIE	SATAPCIE	NC
16	SATAPCIE	SATAPCIE	HDD
17	N/A	SATAPCIE	M2 SSD 2
18	N/A	SATAPCIE	
19	N/A	SATAPCIE	
20	N/A	SATAPCIE	

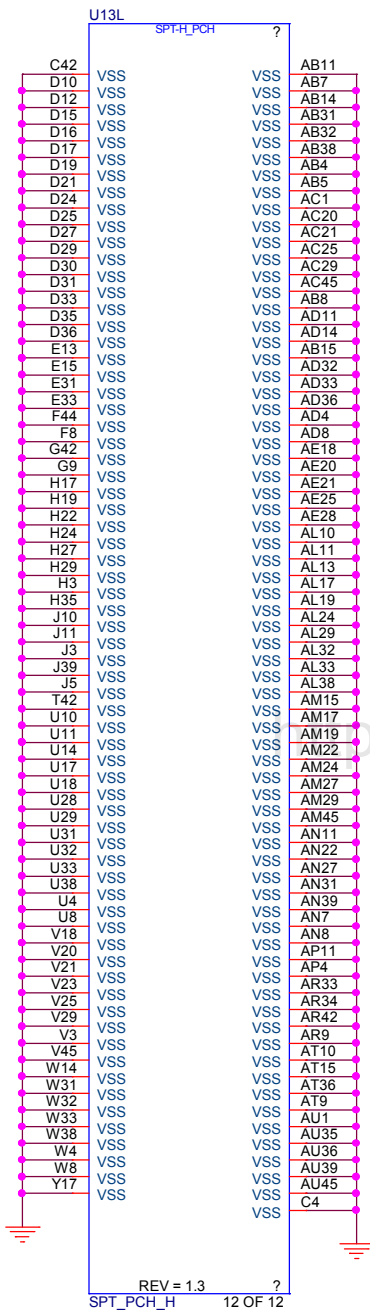
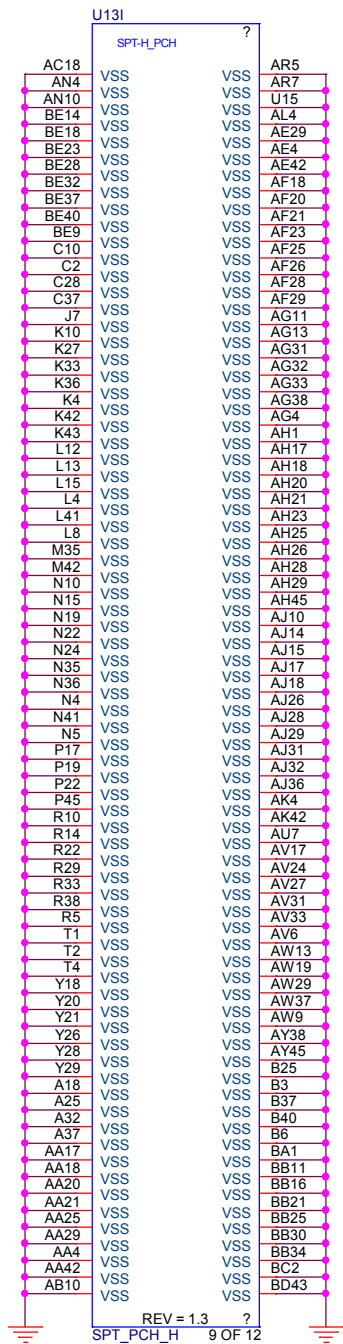


Disable GC6



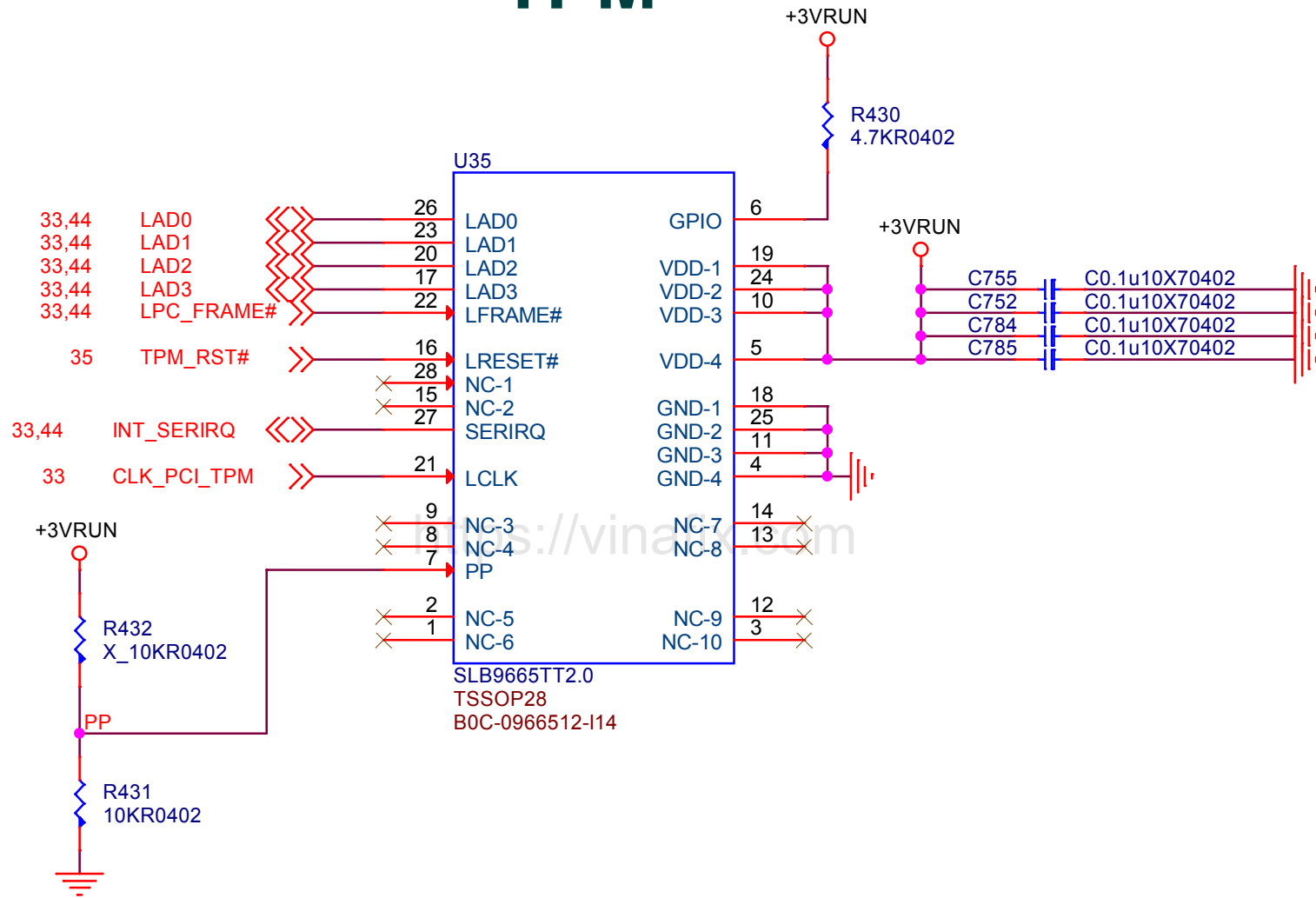


		MICRO-STAR INT'L CO.,LTD.	
Title			
PCH-5 (Power)			
Size	Document Number		Rev
	MS-16H7		1.0
Date:	Thursday, June 04, 2015	Sheet	36 of 74



msi MICRO-STAR INT'L CO.,LTD.		
Title		
PCH-06 (GND)		
Size	Document Number	Rev
	MS-16H7	1.0
Date:	Thursday, June 04, 2015	Sheet 37 of 74

TPM



MICRO-STAR INT'L CO.,LTD.

Title

TPM

Size

Document Number

MS-16H7

Rev

1.0

Date:

Thursday, June 04, 2015

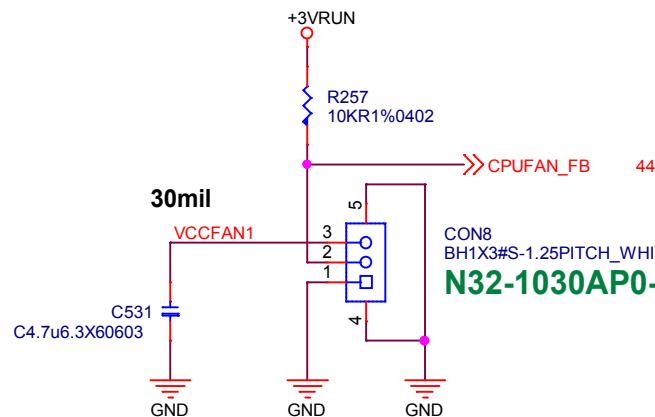
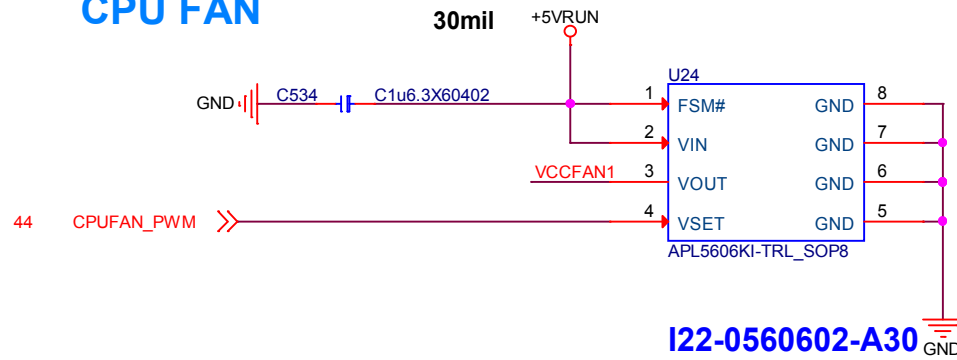
Sheet

38

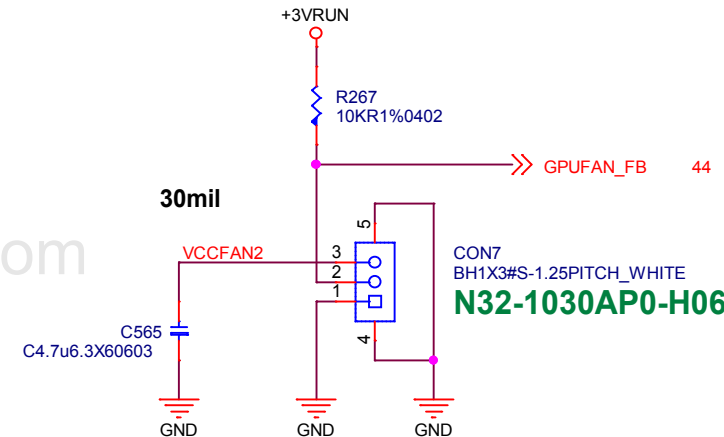
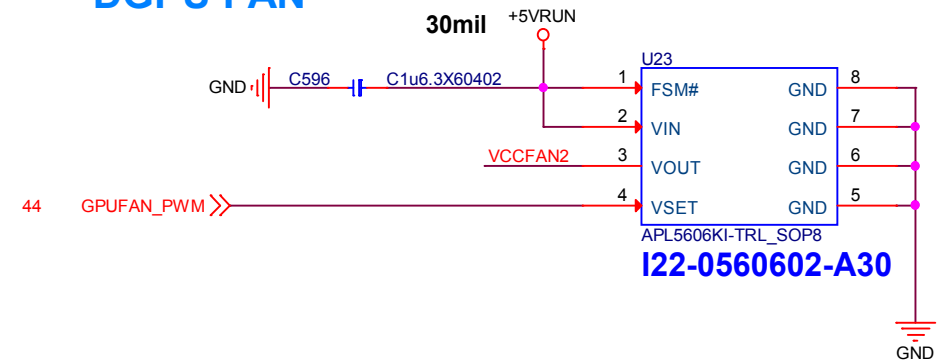
of

74

CPU FAN



DGPU FAN



msi

MICRO-STAR INT'L CO.,LTD.

Title

CPU FAN/DGPU FAN

Size

Document Number

MS-16H7

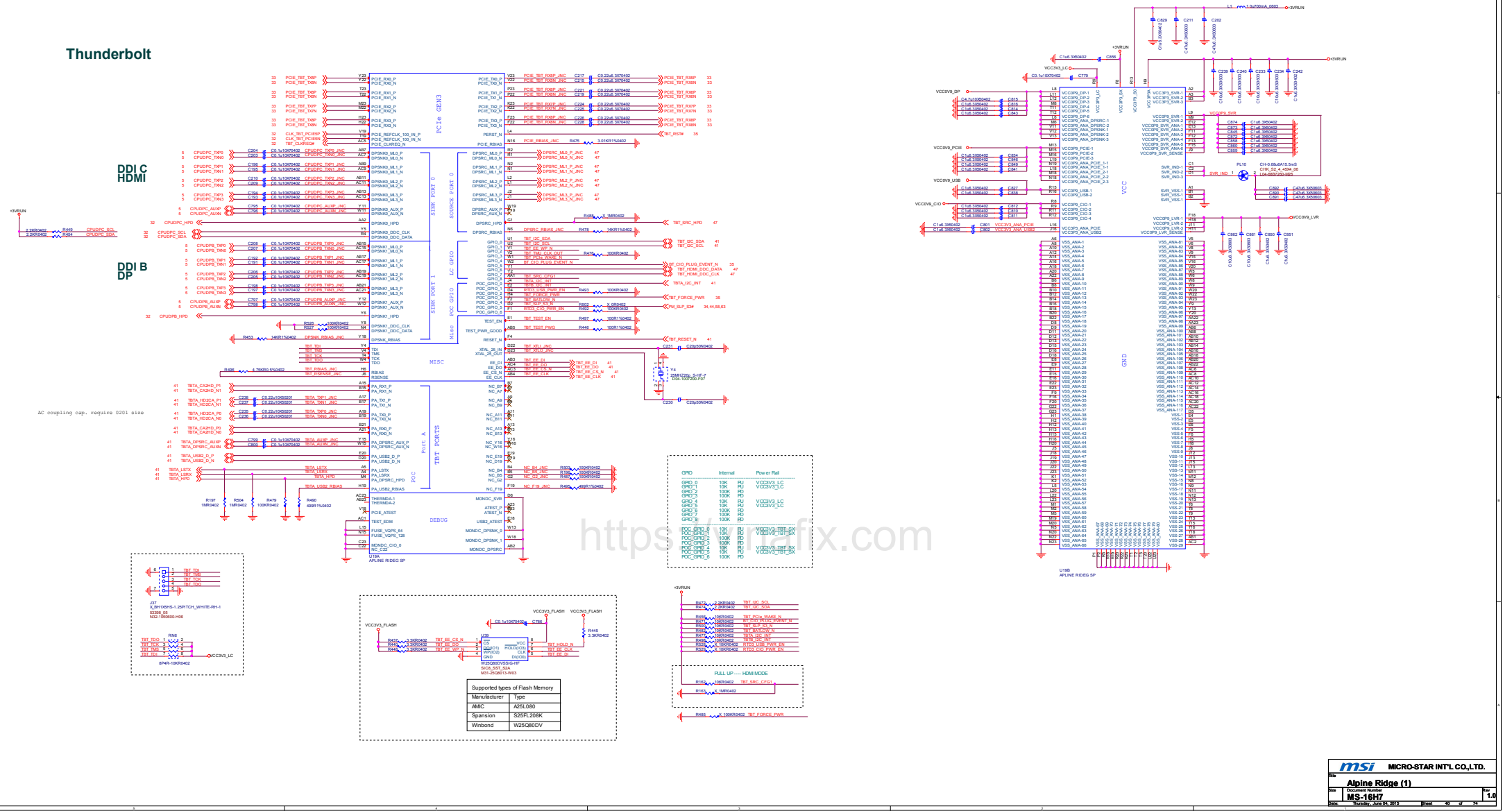
Rev

1.0

Date: Thursday, June 04, 2015

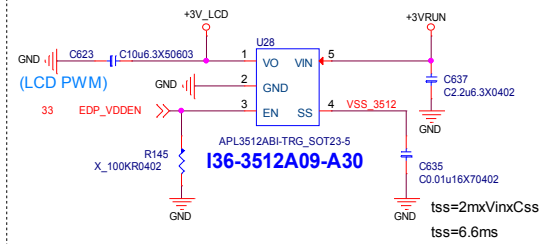
Sheet 39 of 74

Thunderbolt

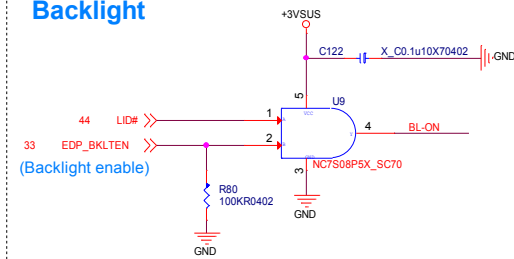


eDP Connector

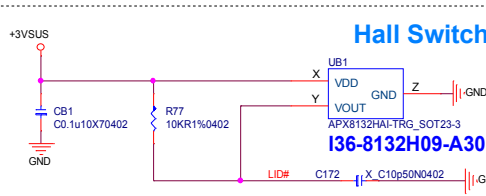
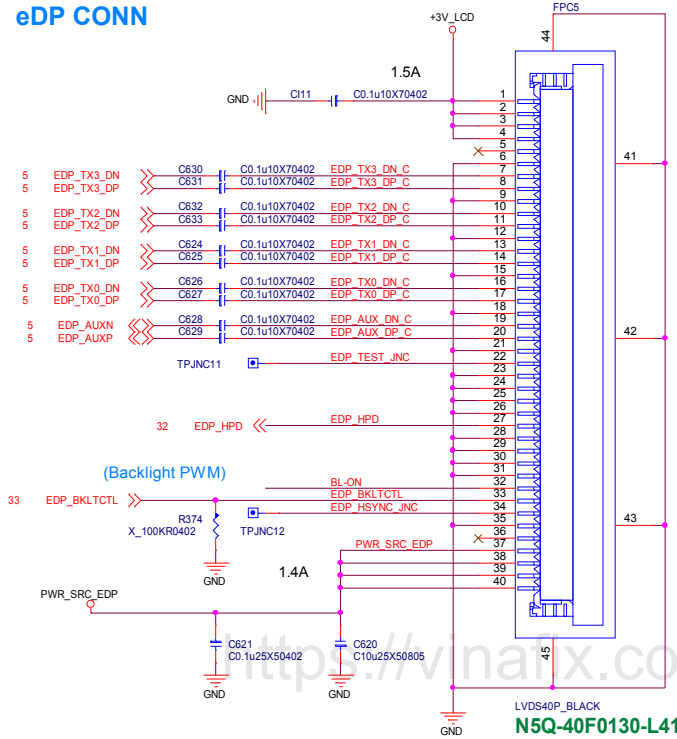
Panel Device Logic Power



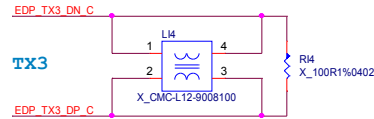
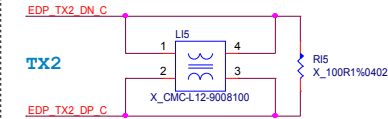
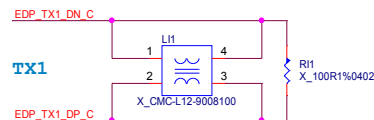
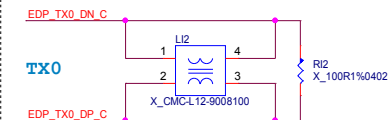
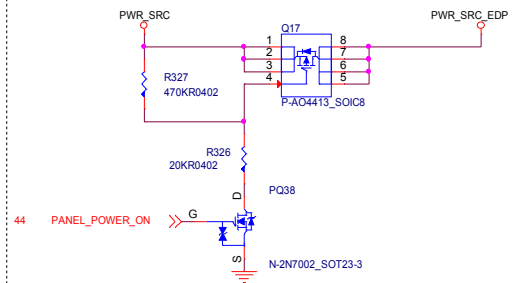
Backlight



eDP CONN

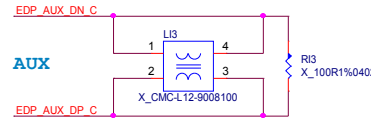


Panel Power



Place Close eDP Connector

Reserve for EMI

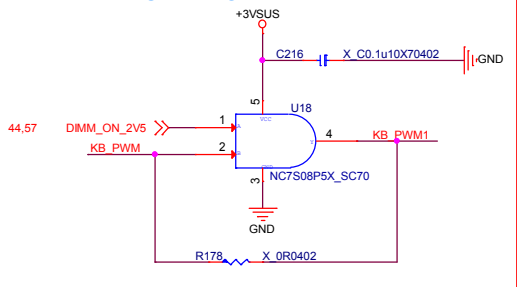


LCD Module Pin Define

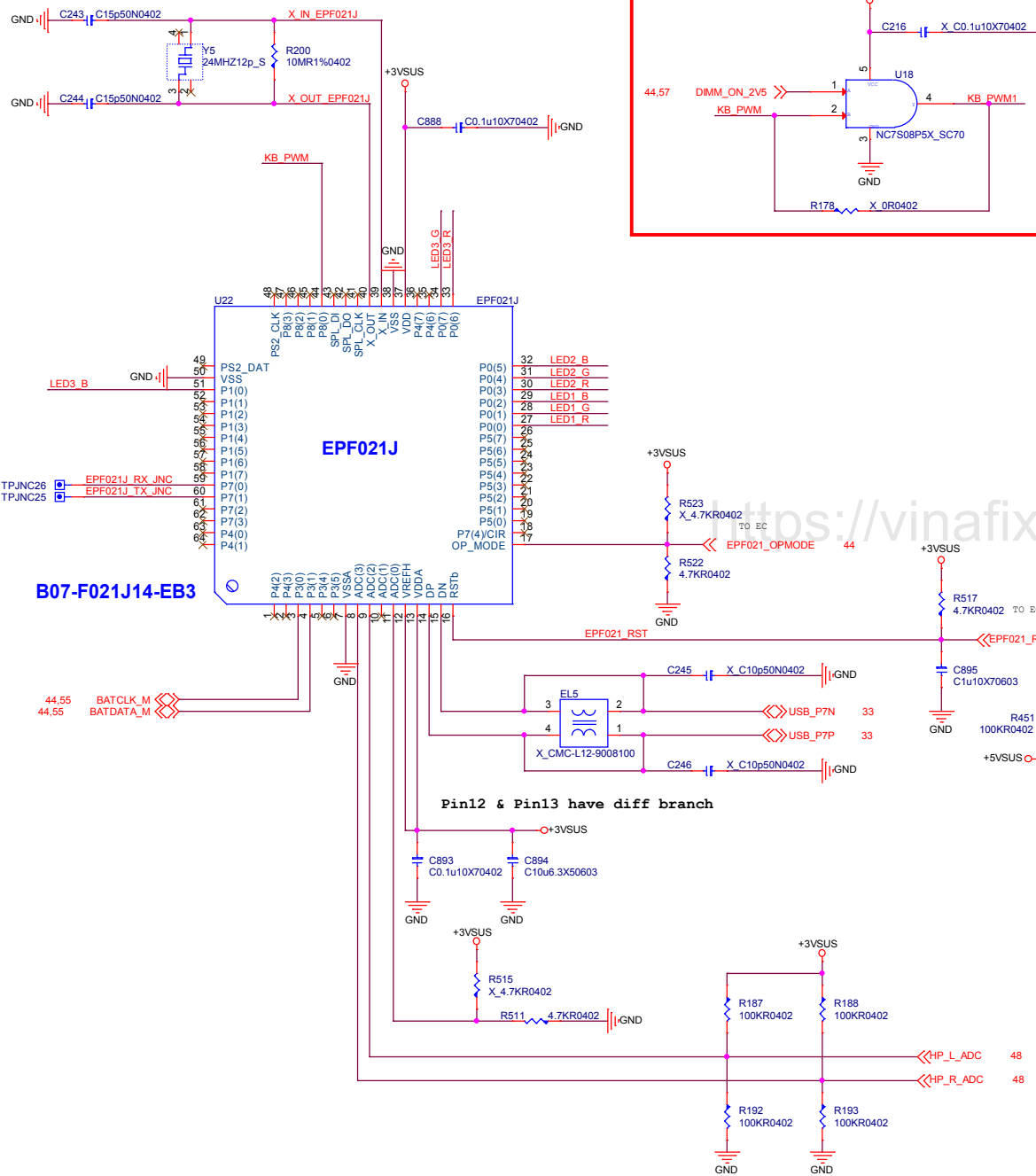
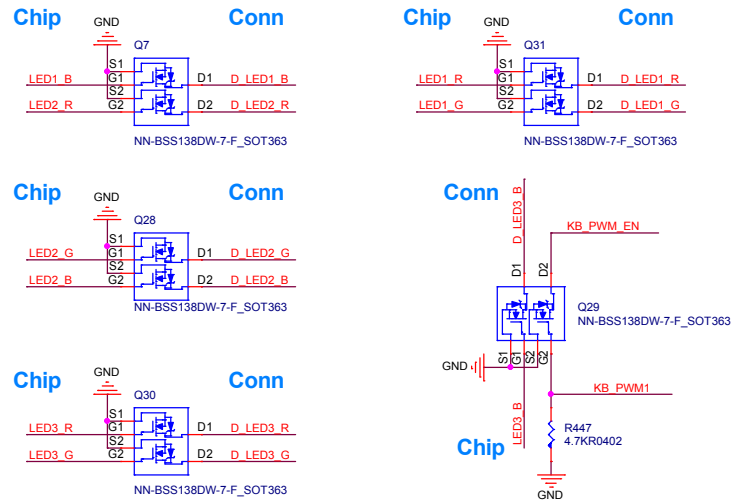
Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPDP signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

LED Driver IC(EPF021J)

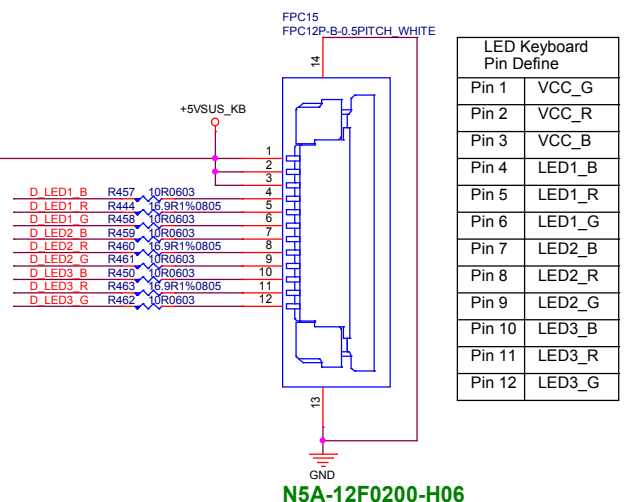
LED KB FLASH ERROR



EPF021J Sink current not enough, only using BSS138 (0.22A)



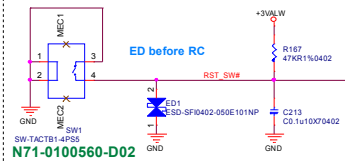
LED Keyboard CONN



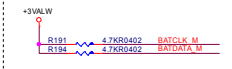
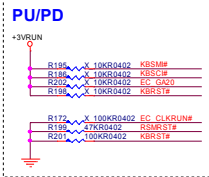
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC/EC/uP (ENE9028)

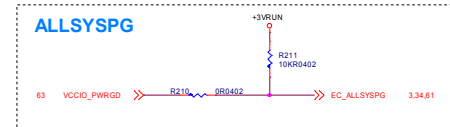
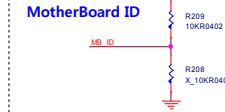
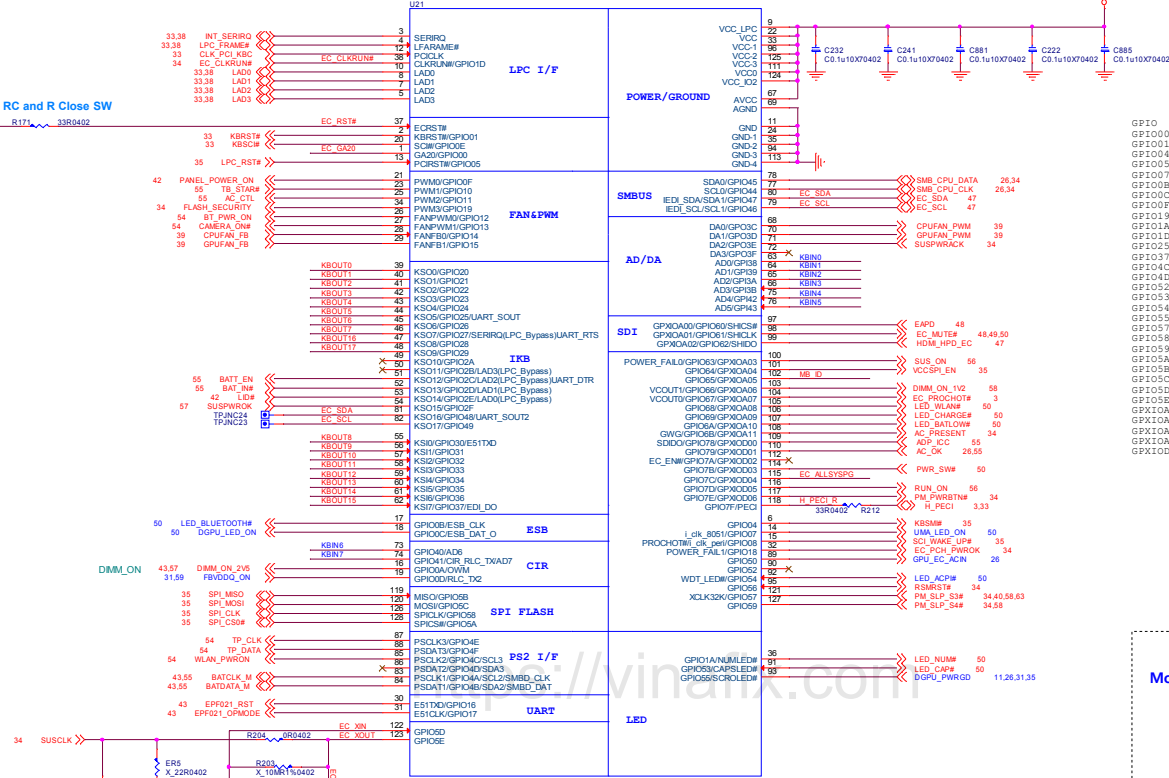
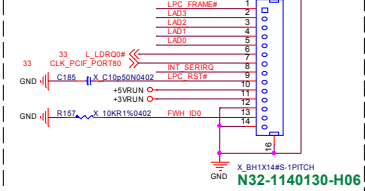
Hardware Reset



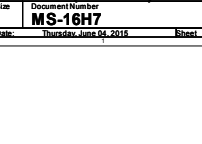
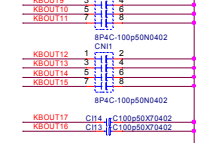
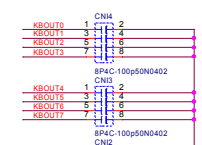
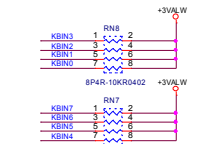
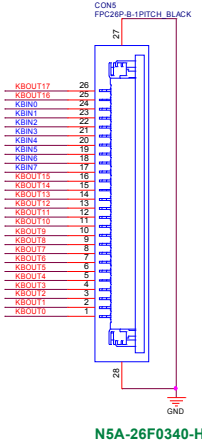
RSMRST# follow DG modify to 10K



SW Debug (LPC)



Keyboard conn



CardReader (RTS5249)

Power Trace

Pin11(3V3_IN) / Pin 12(CARD_3V3)trace fixed width is 40 mils (minimum)

Pin27(3V3aux) / Pin 13(SD_VDD2)trace fixed width is 30 mils (minimum)

Pin10(AV12) / Pin 14(DV12S) / Pin 18(DV33_18) / Pin 24(SDREG2) trace fixed width is 20 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

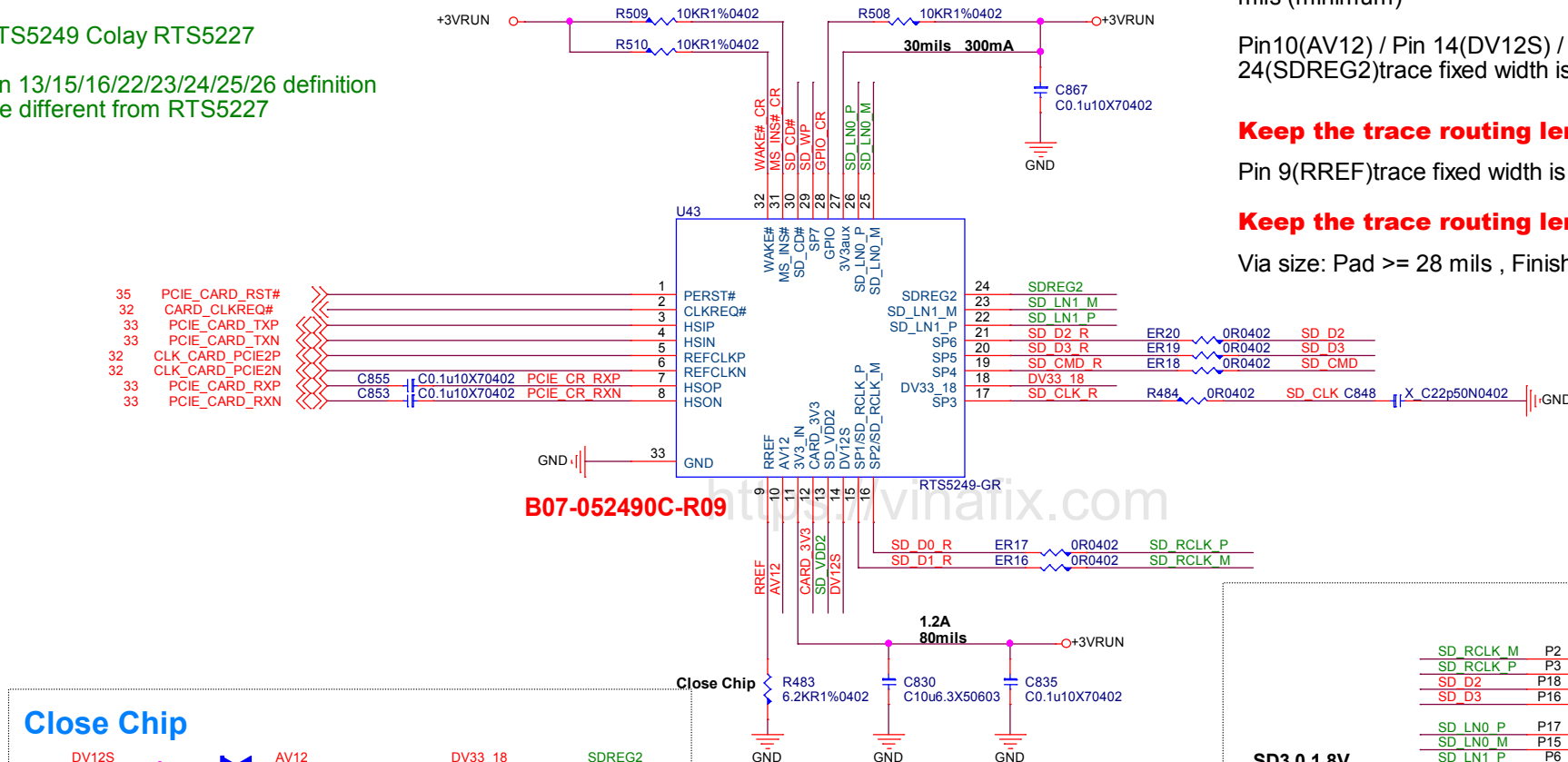
Pin 9(RREF)trace fixed width is 12 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

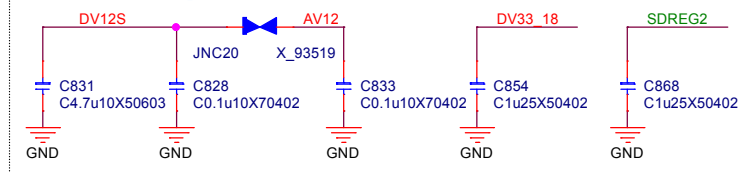
Via size: Pad ≥ 28 mils , Finished hole ≥ 16 mils.

RTS5249 Colay RTS5227

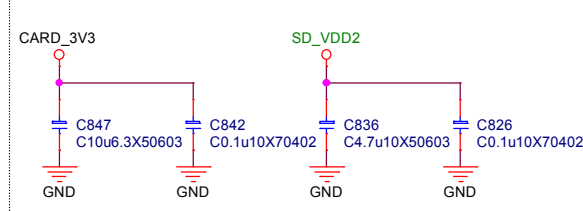
Pin 13/15/16/22/23/24/25/26 definition
are different from RTS5227



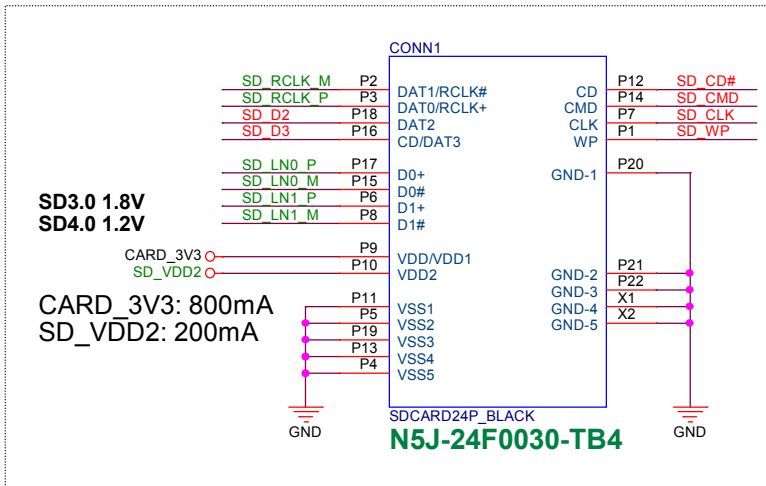
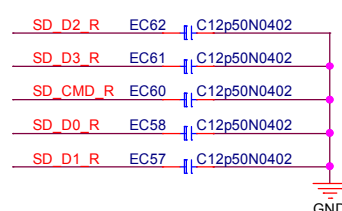
Close Chip



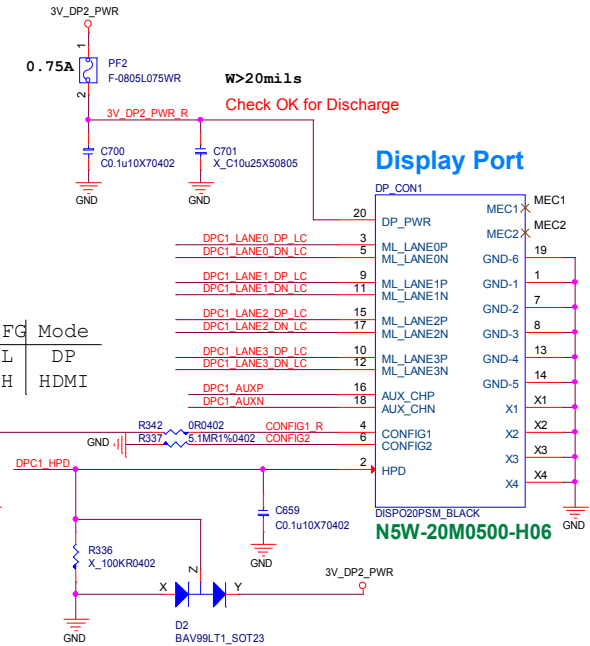
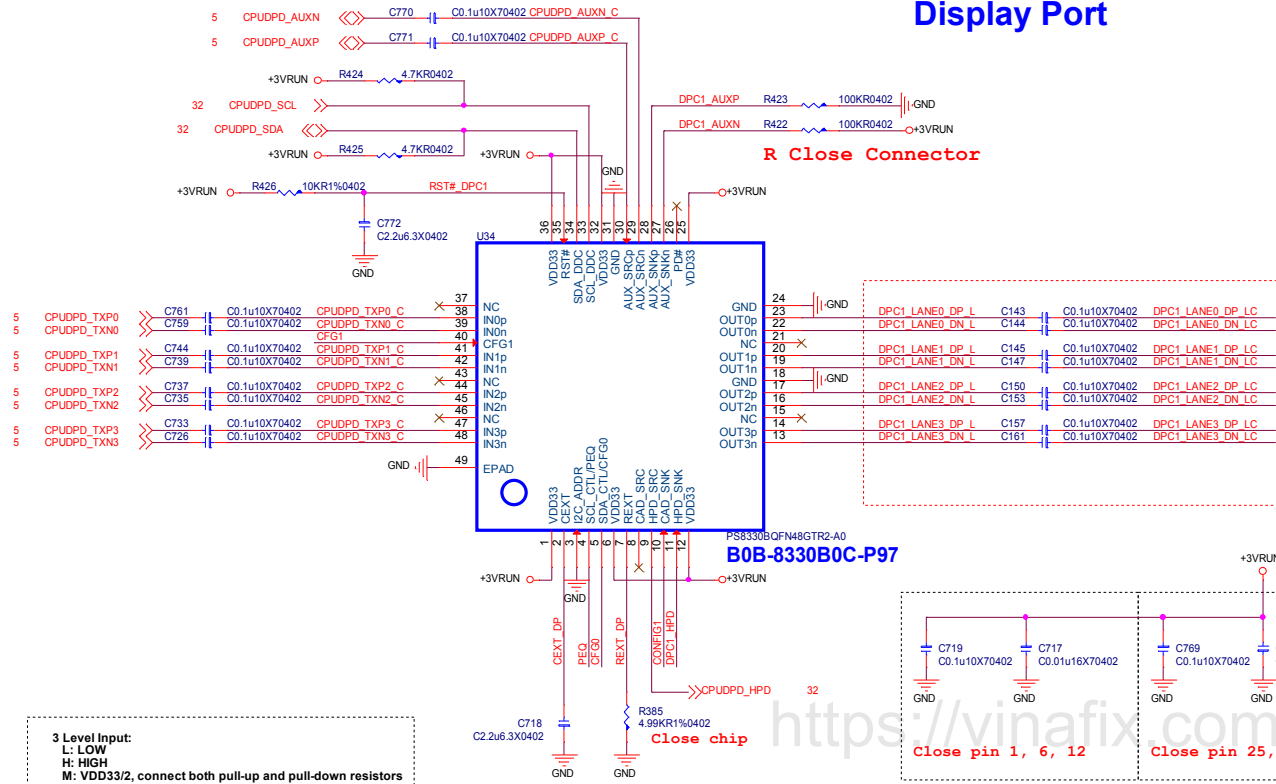
Close Connector



EMI

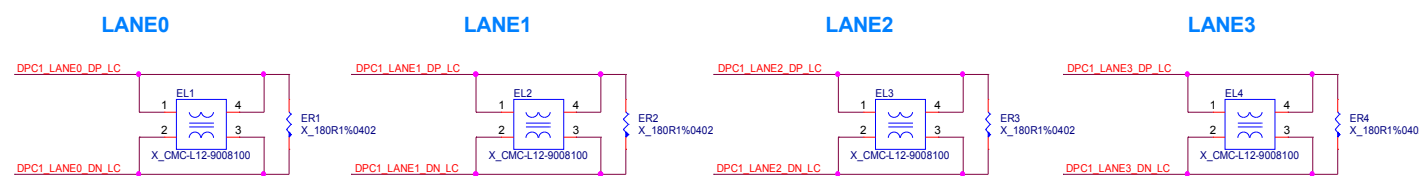


Display Port

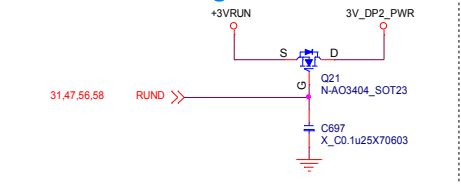


CAD_SNK Have internal Pull down 1Mohm.
HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

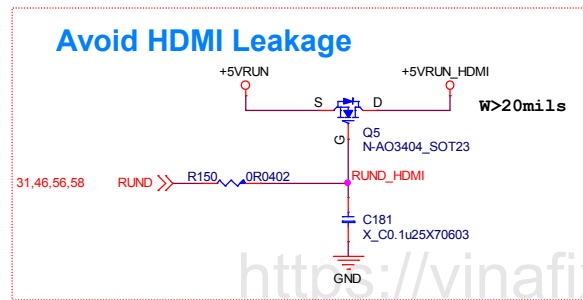
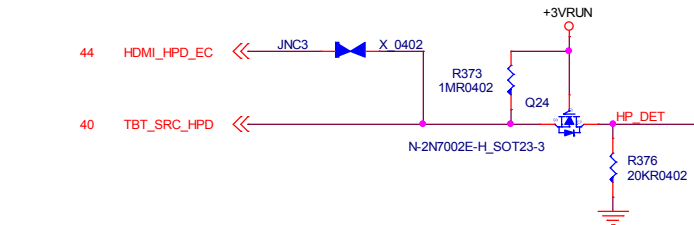
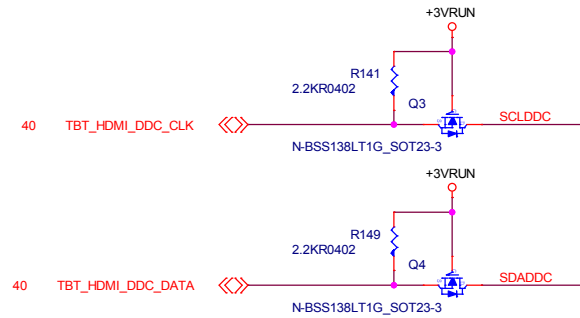
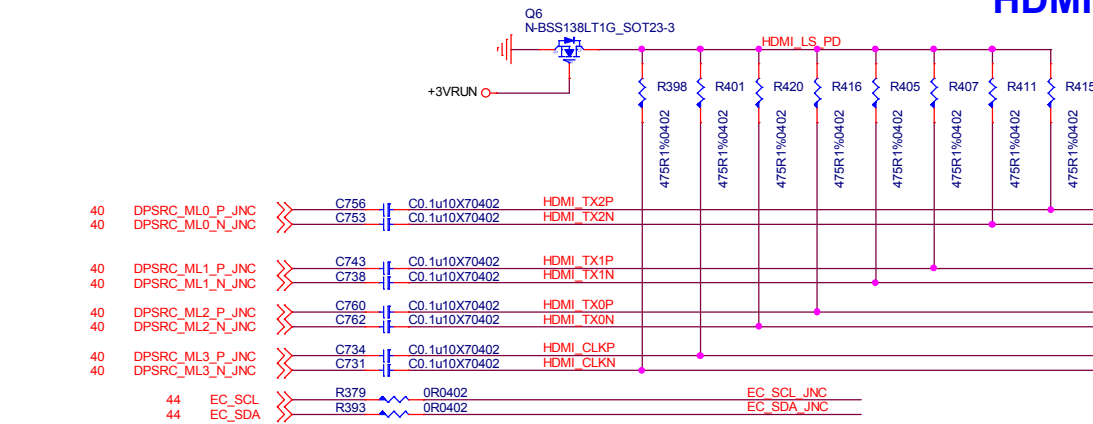
EMI Close Connector



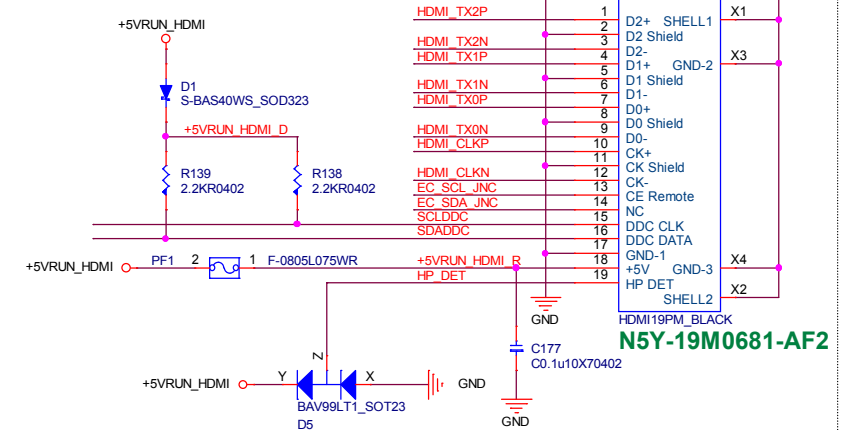
Avoid DP Leakage



HDMI Repeater

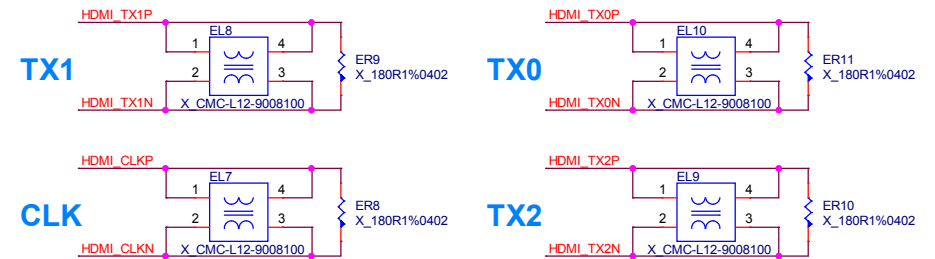


HDMI Connector



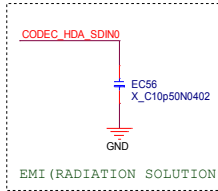
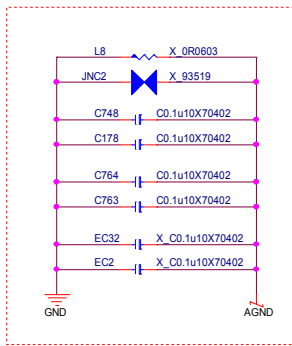
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

EMI Close Connector

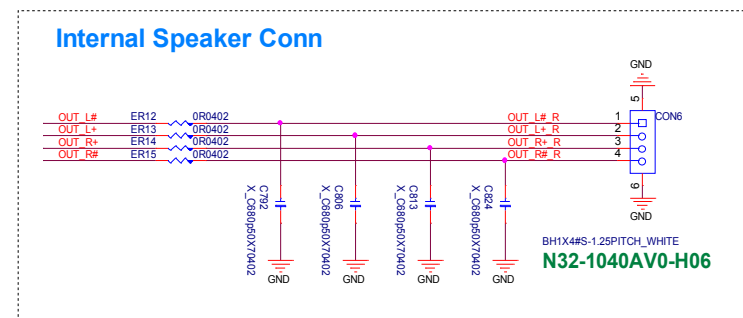
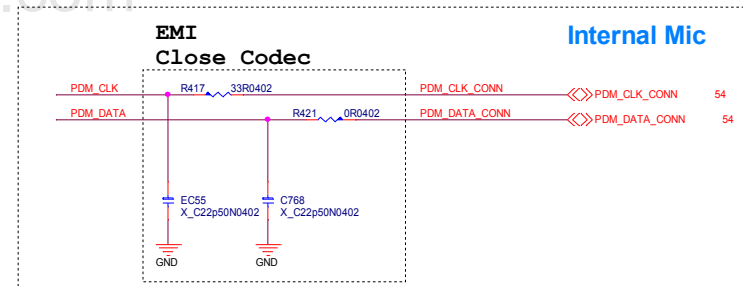
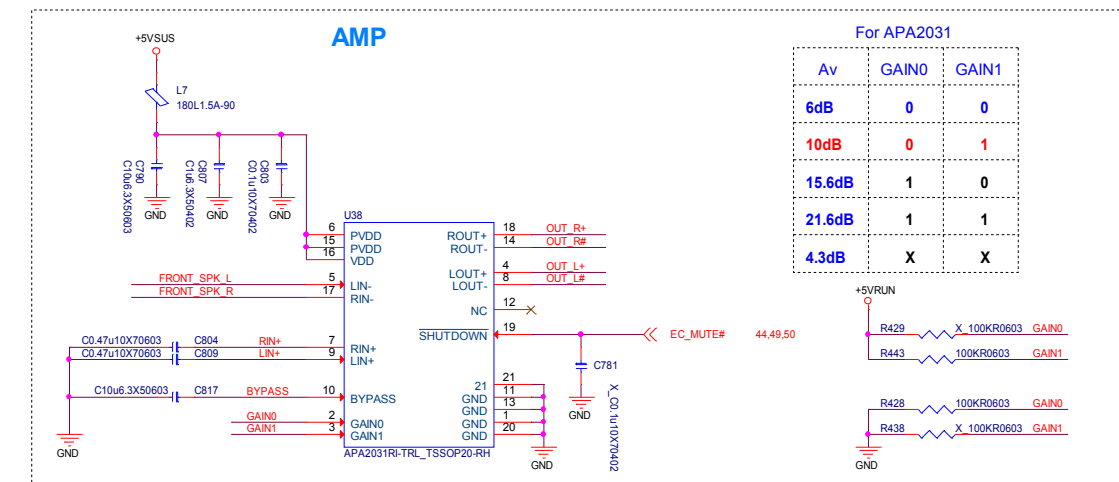
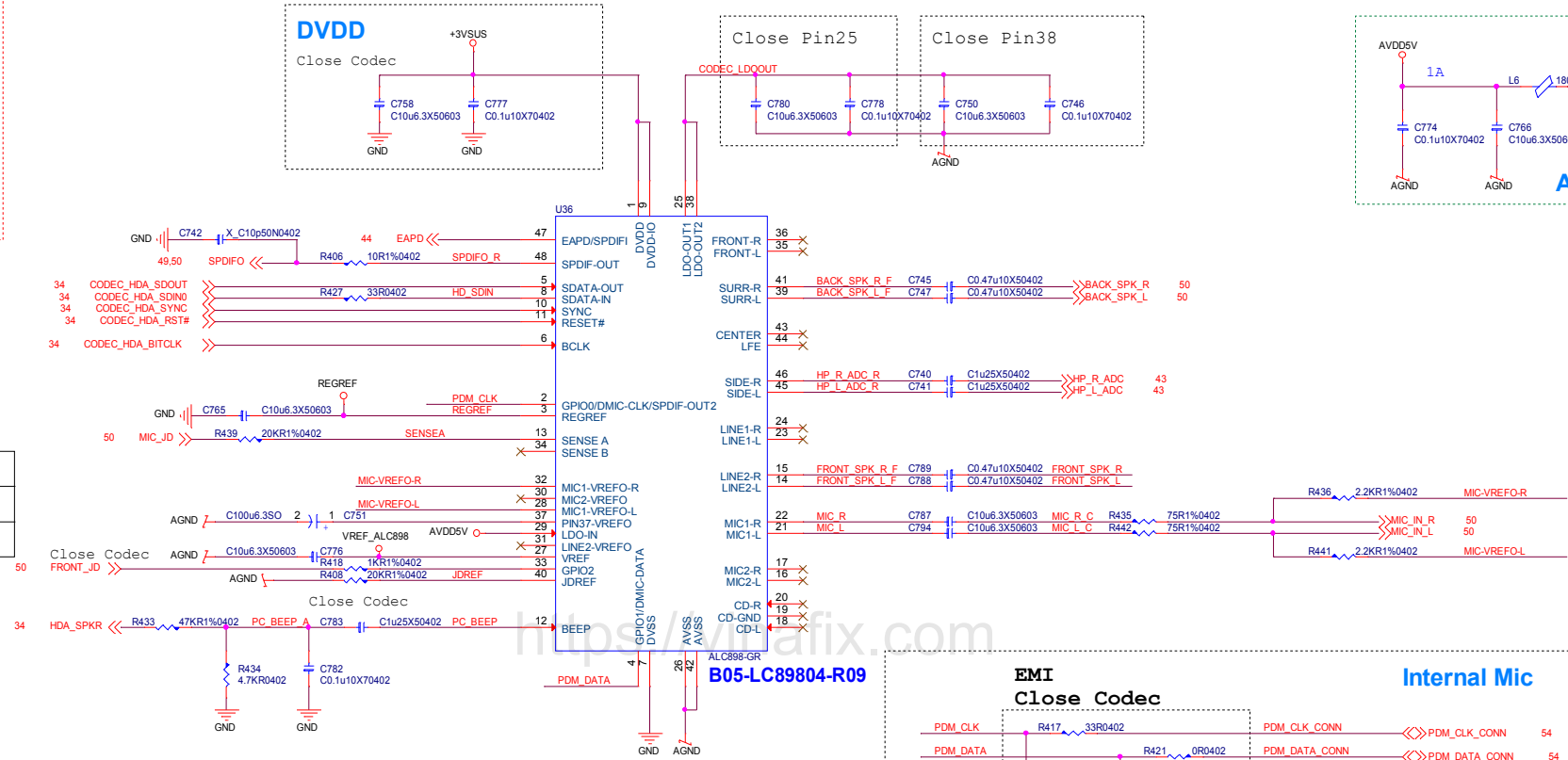


msi MICRO-STAR INT'L CO.,LTD.	
Title	
HDMI Repeater	
Size	Document Number
MS-16H7	
Date:	Thursday, June 04, 2015
Sheet	47 of 74
Rev	1.0

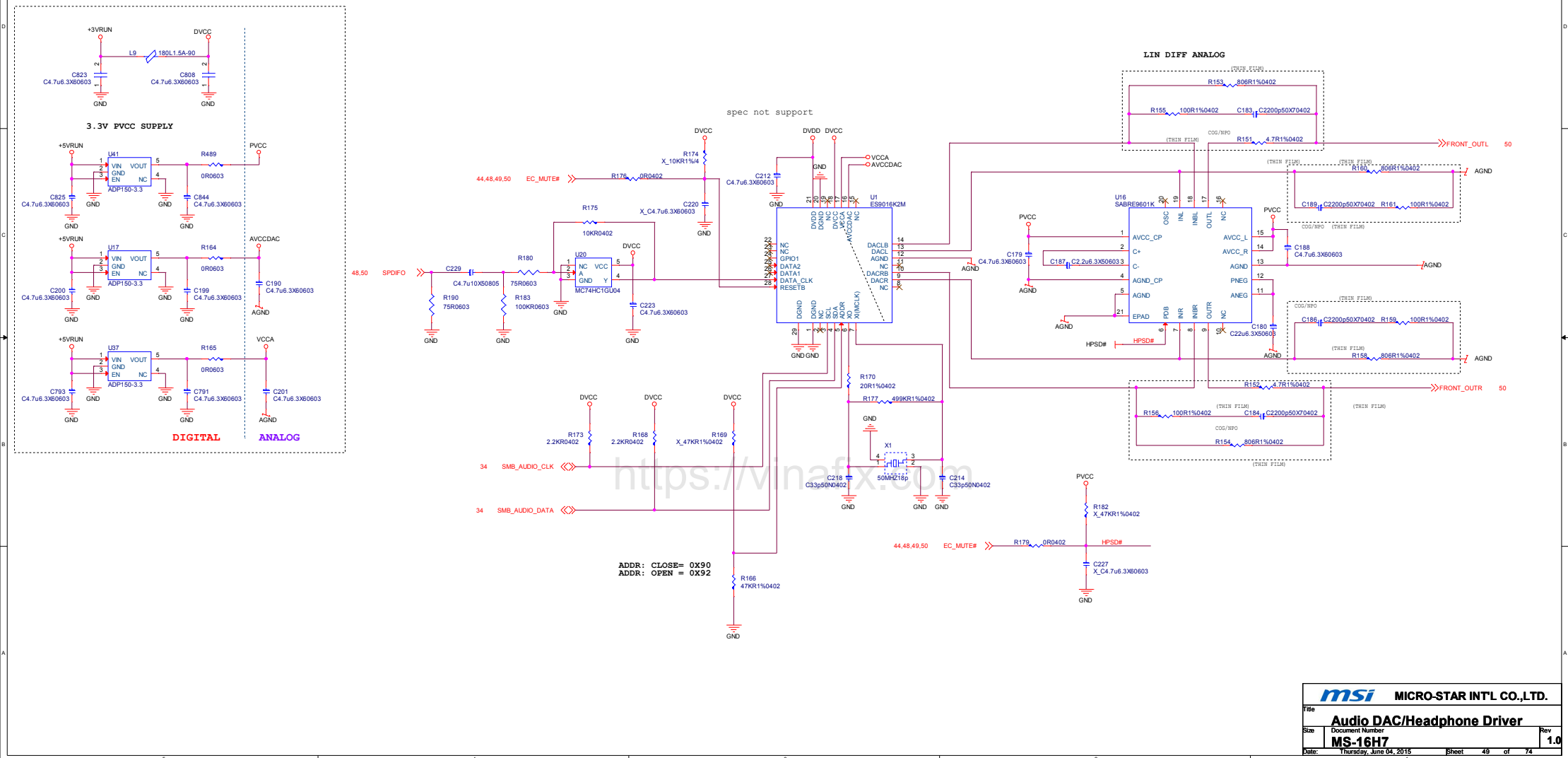
Audio CODEC(ALC898/ALC892)/Audio AMP(APA2031)



PIN 37 - VREFO	
ALC892	NC
ALC898	Stuff

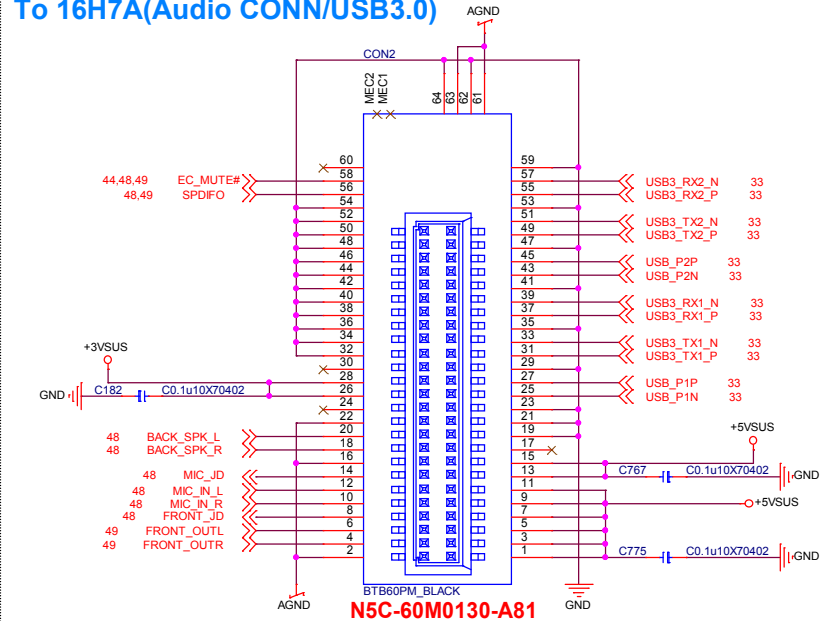


Audio DAC(ES9018)/Headphone Driver(SABRE9601)

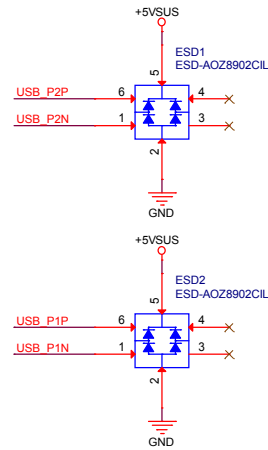


BTB CONN

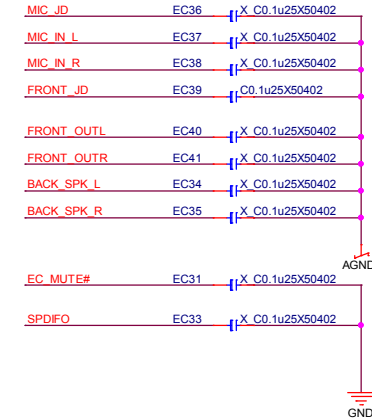
To 16H7A(Audio CONN/USB3.0)



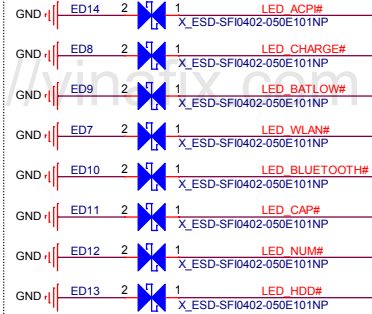
ESD



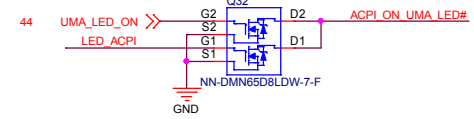
EMI



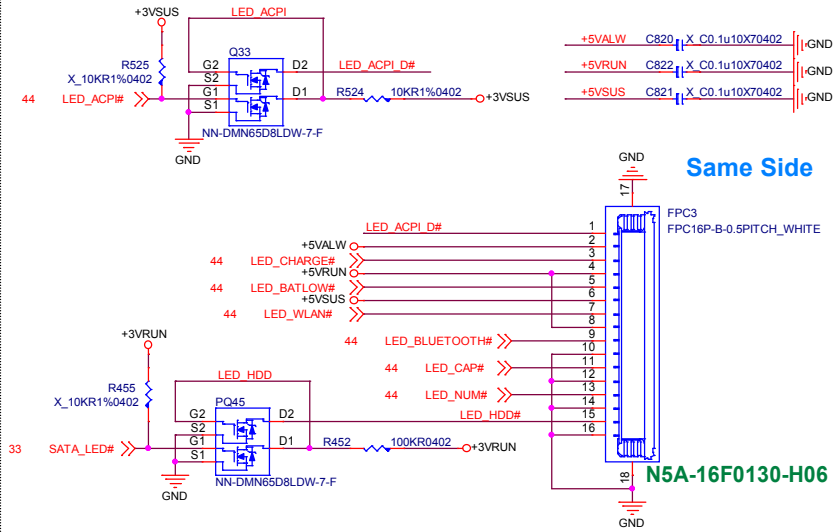
EMI



S3 Breath S0 No active

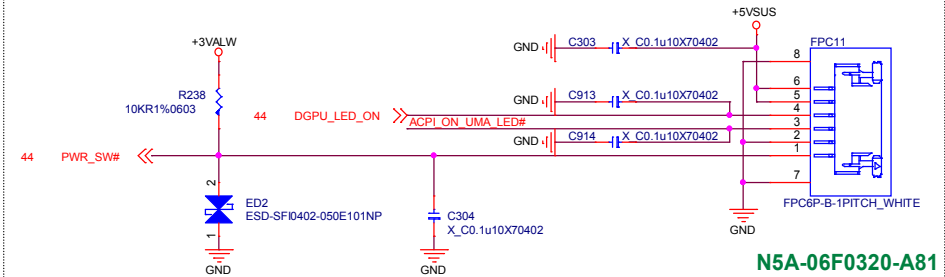


To 16H7B(LED Board)

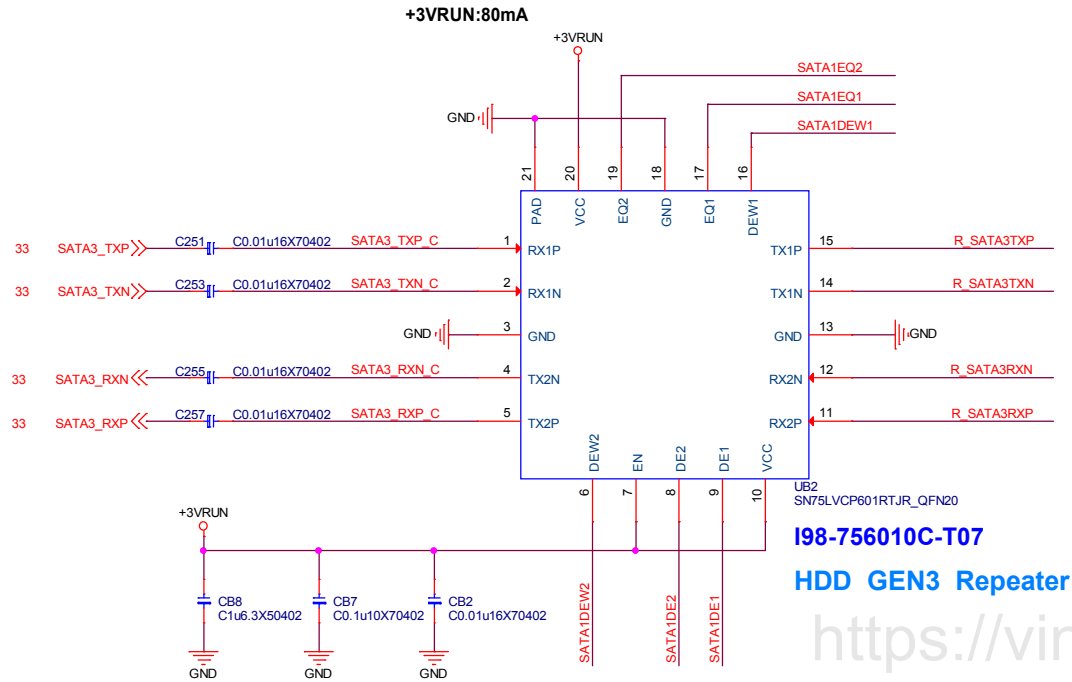


Same Side

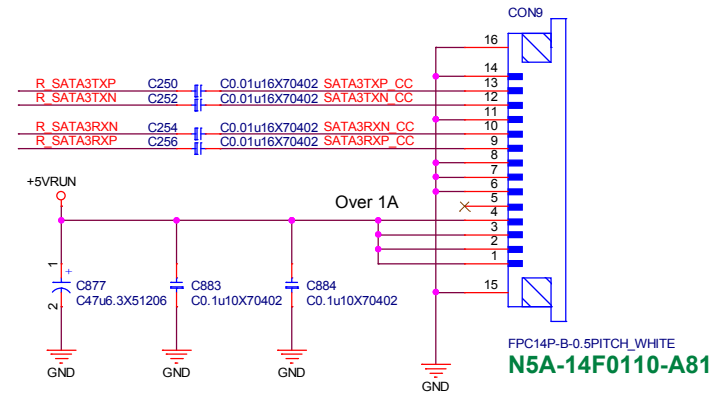
To 16H7C (Power Board)



HDD (With Repeater)



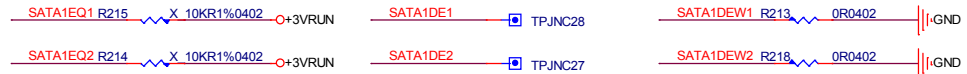
BTB Connector



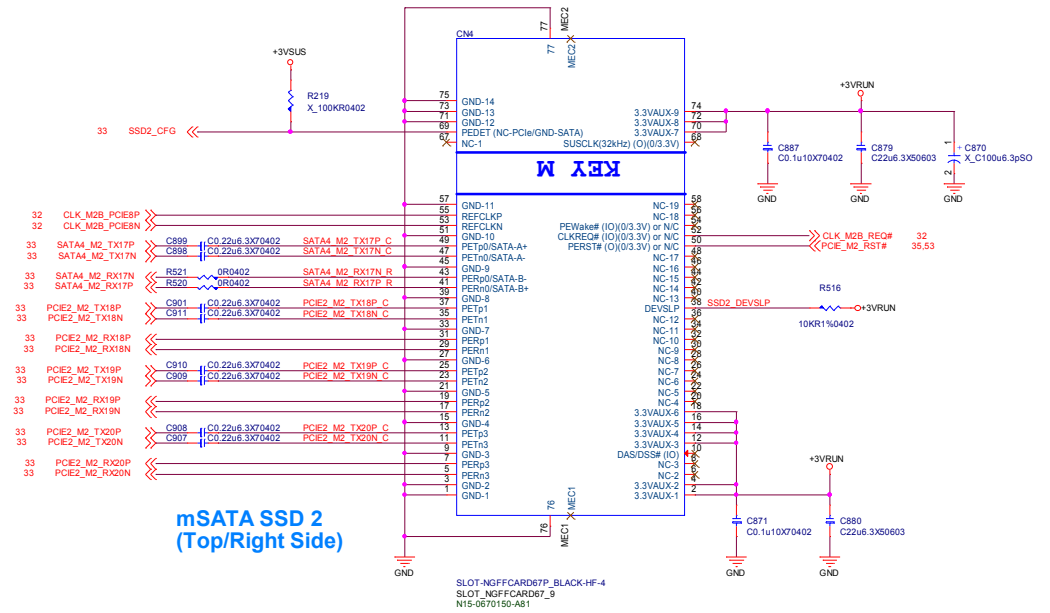
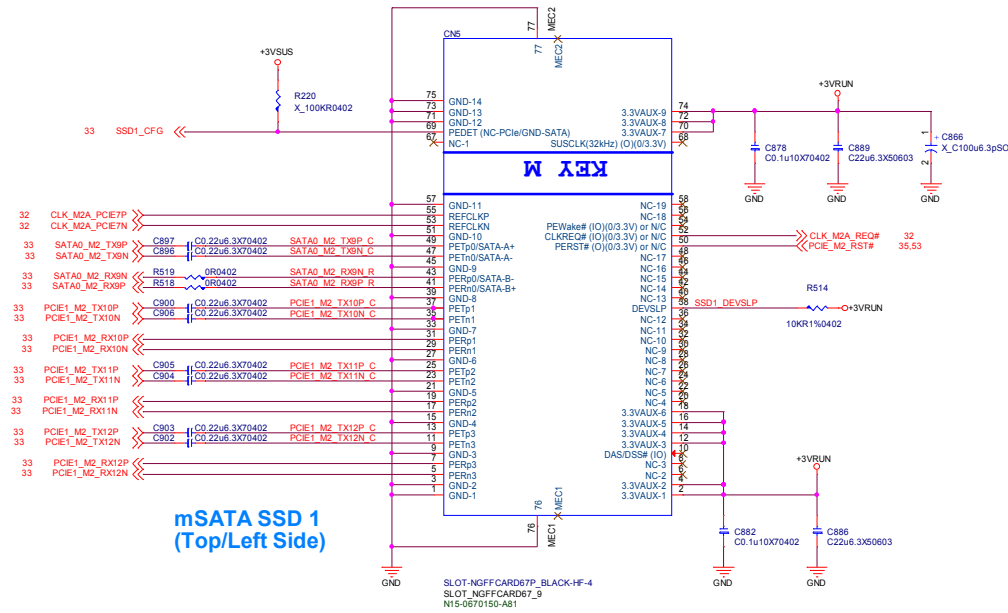
TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1 (default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

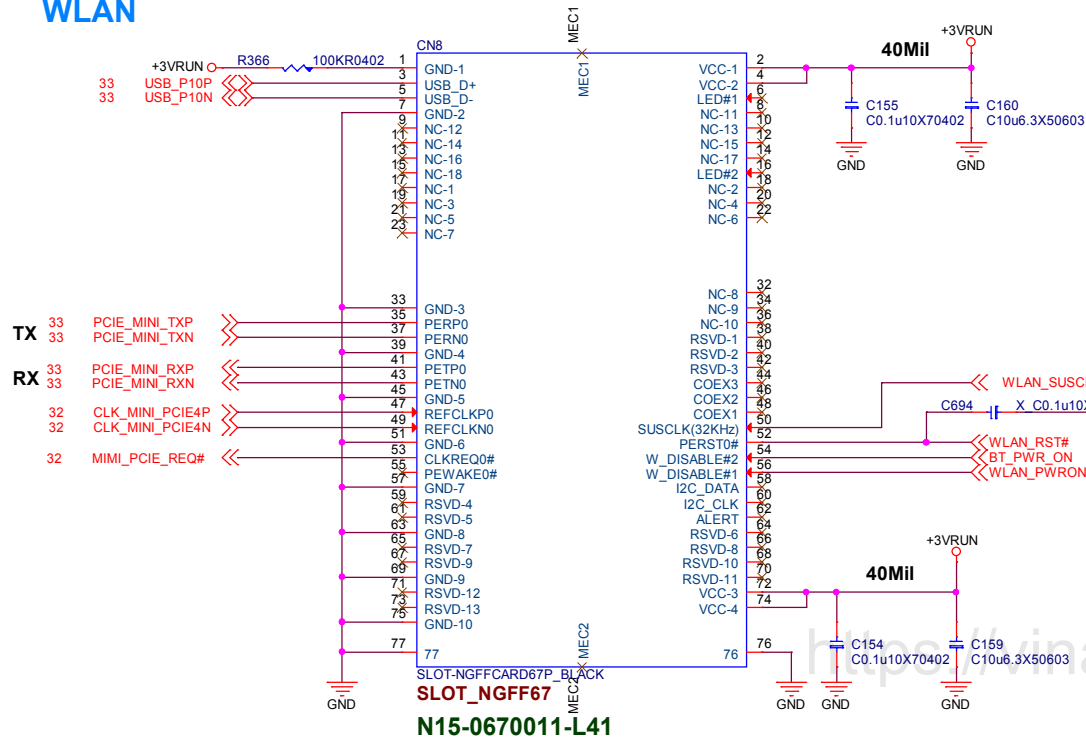


SSD

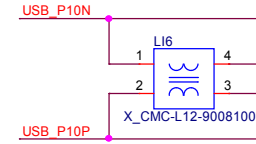


<https://vinafix.com>

WLAN

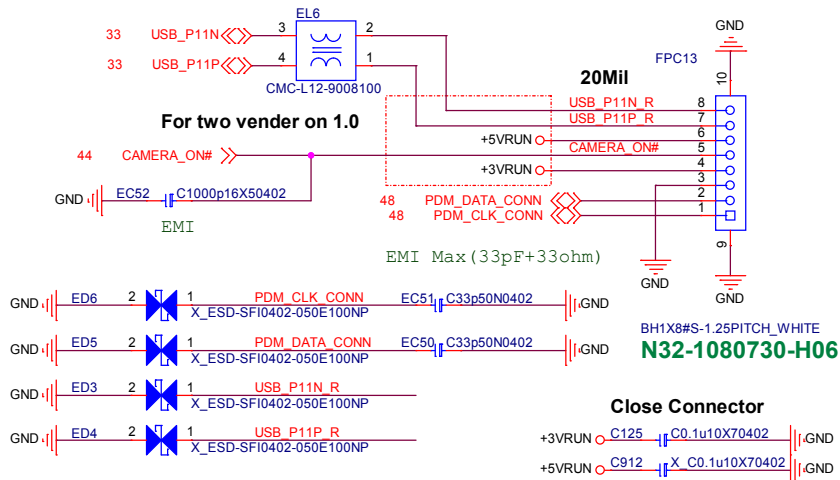


EMI

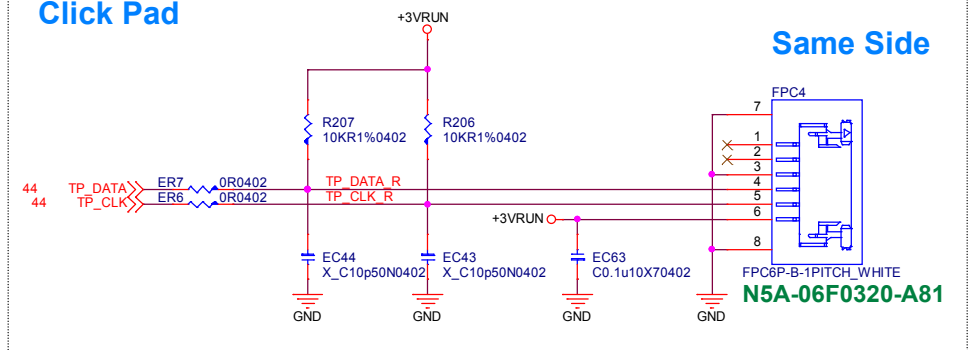


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Click Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	VL_ZN_EN (W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

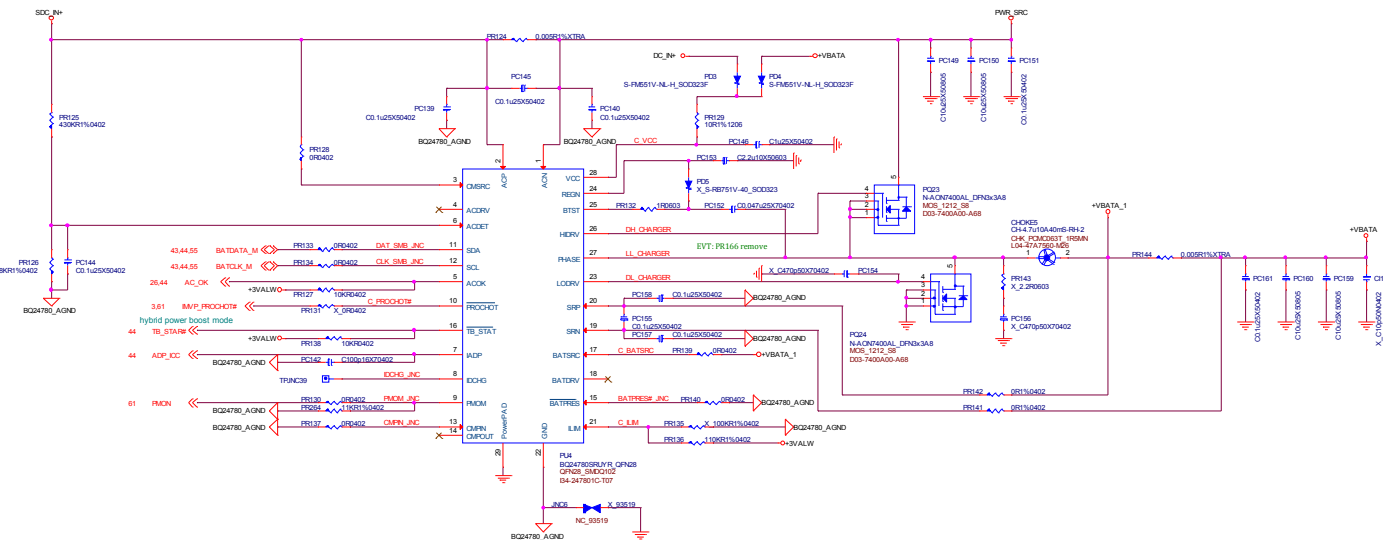
CAMERA



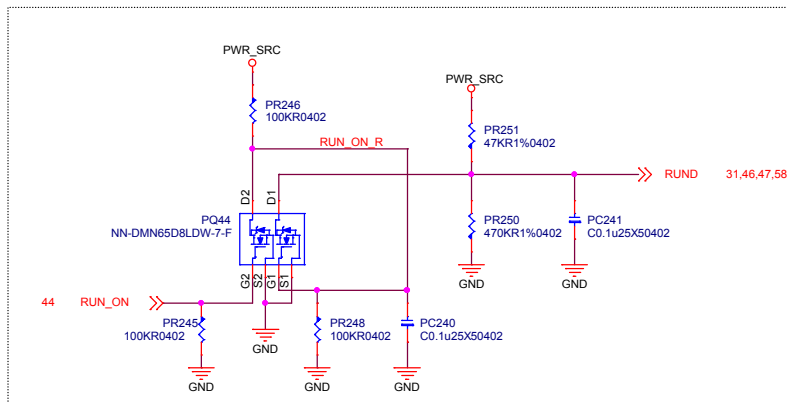
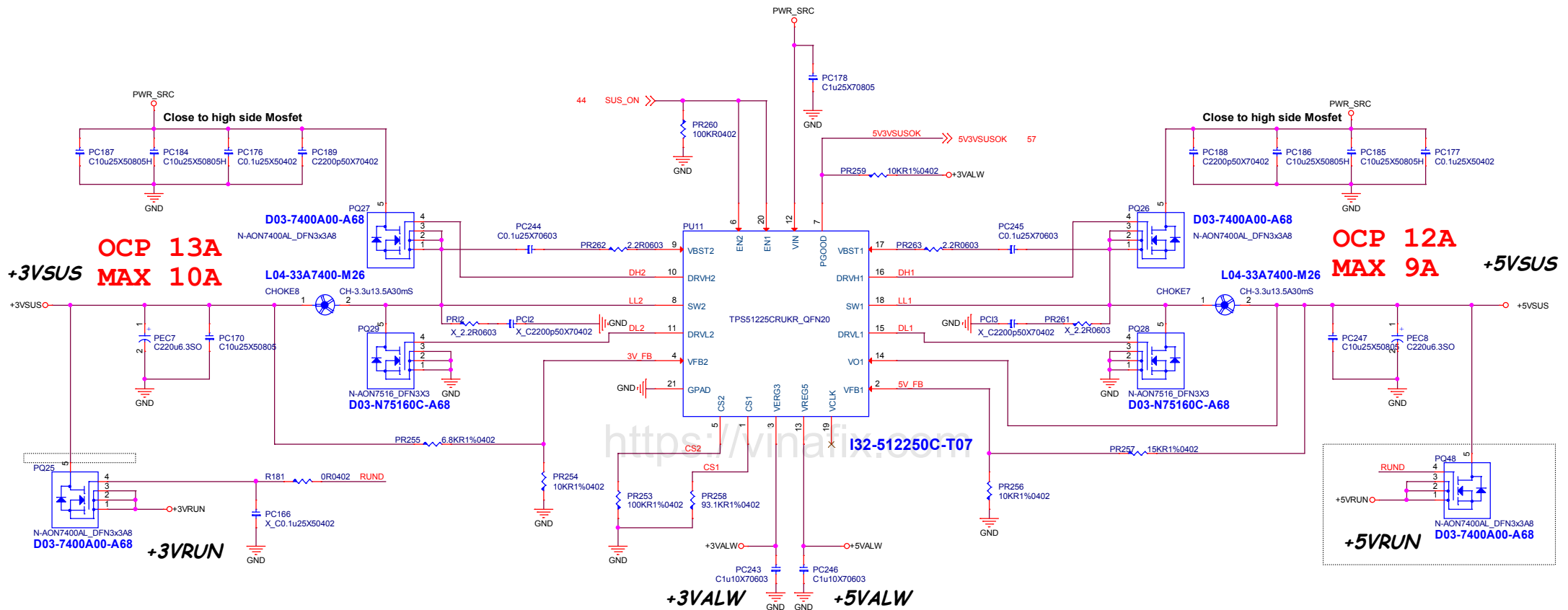
Click Pad



Battery Select

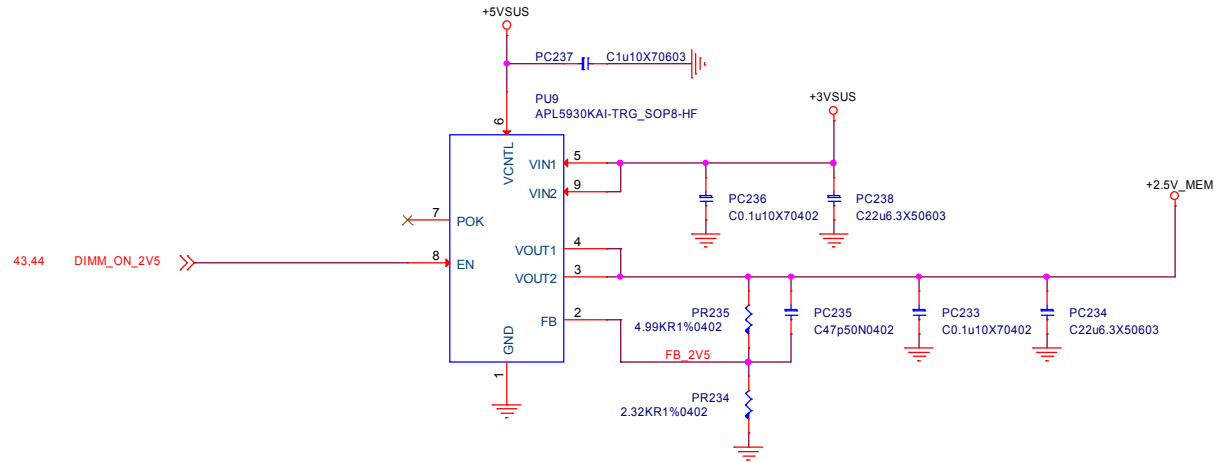


System Power

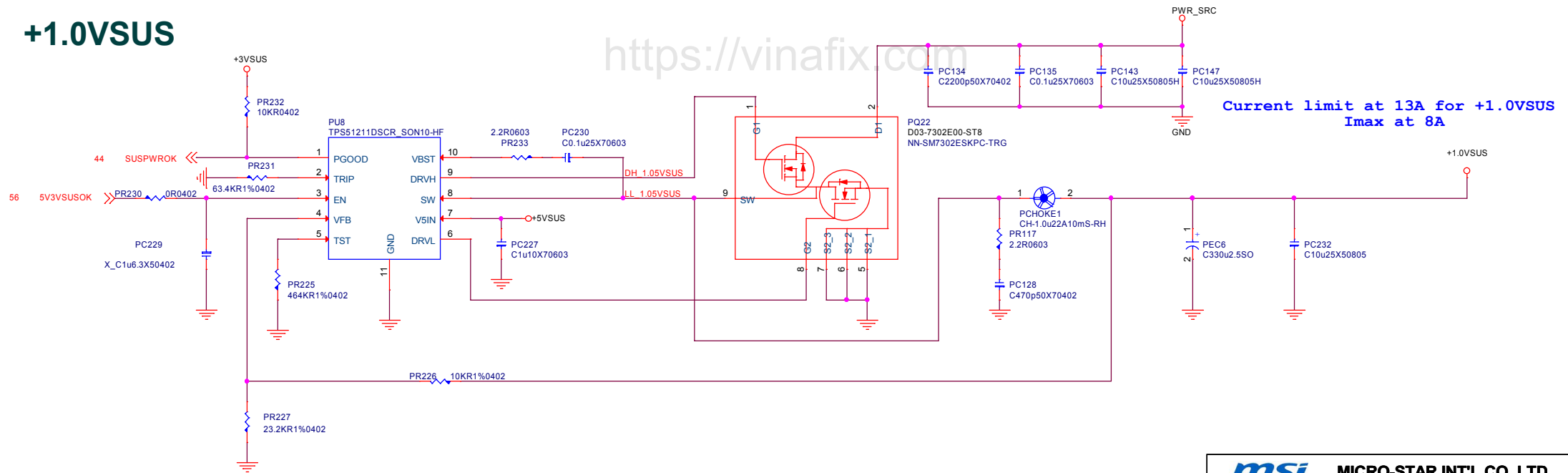


+2.5V_MEM

OCP 4.2A
MAX 1A

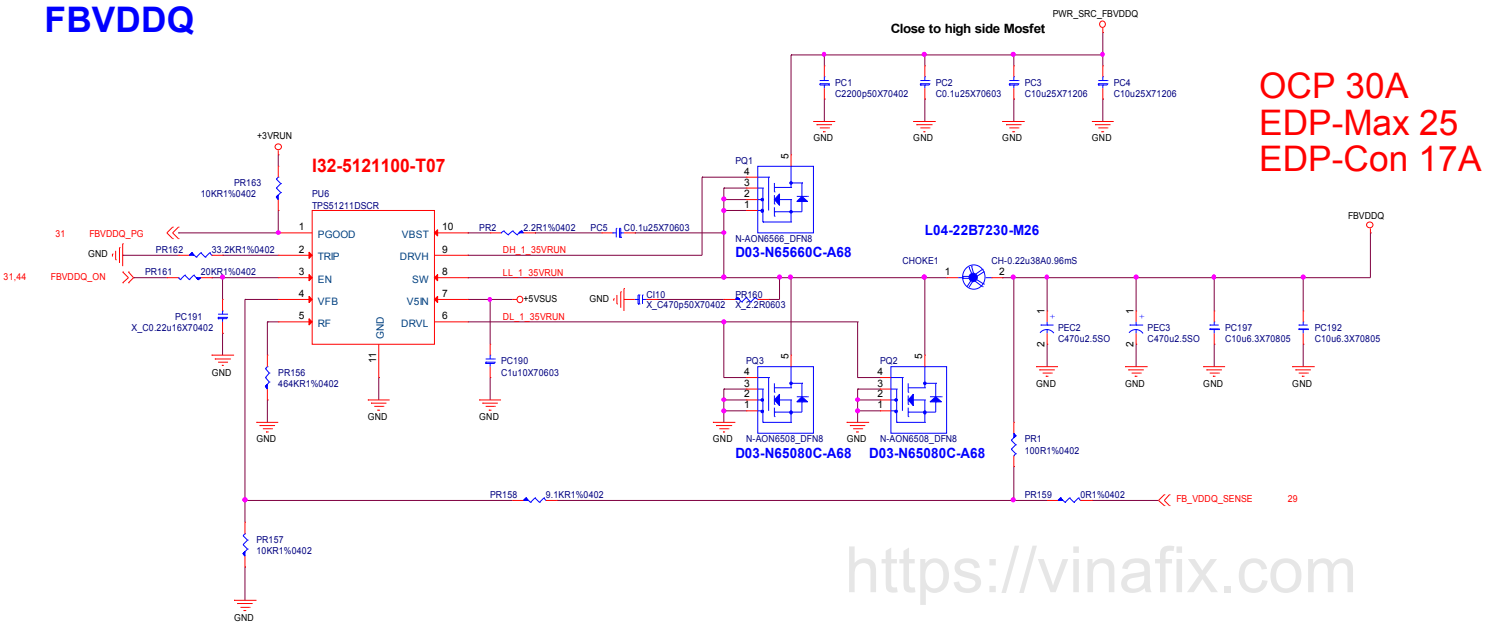


+1.0VSUS



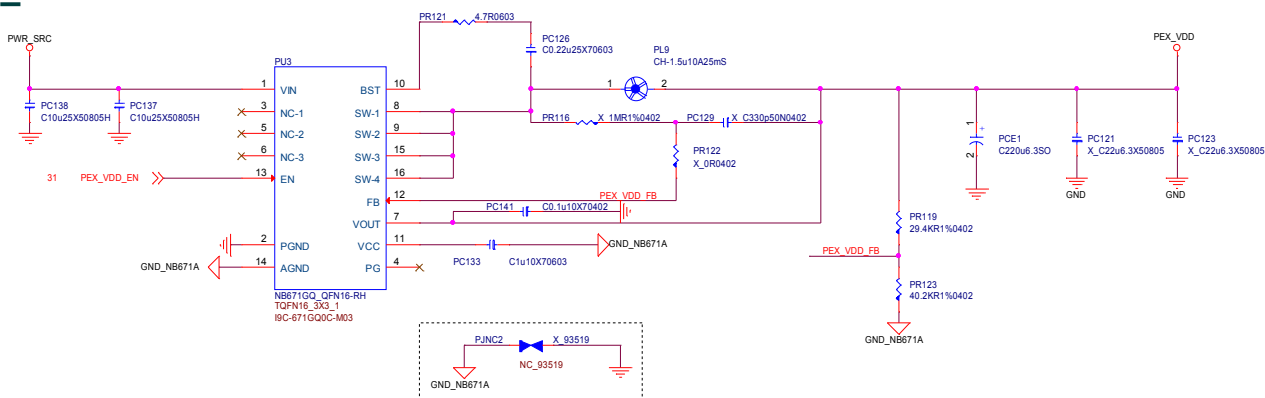
DGPU POWER FBVDDQ

FBVDDQ



PEX_VDD

Imax at 4A

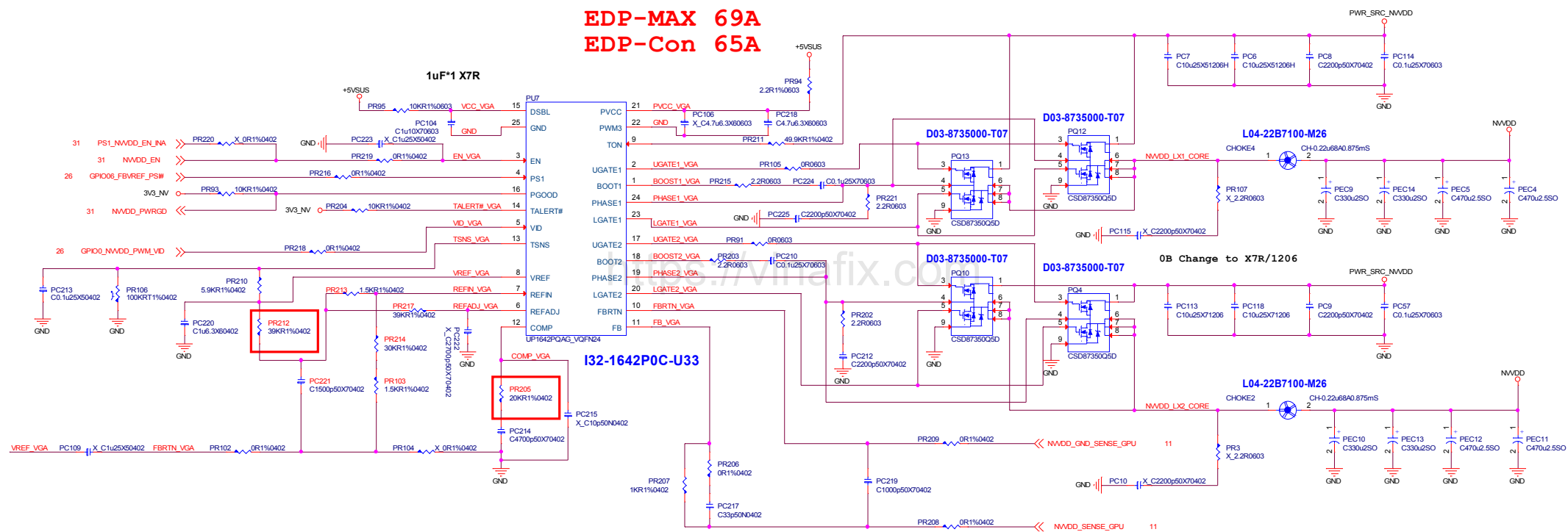


DGPU POWER / UP1642PQAG

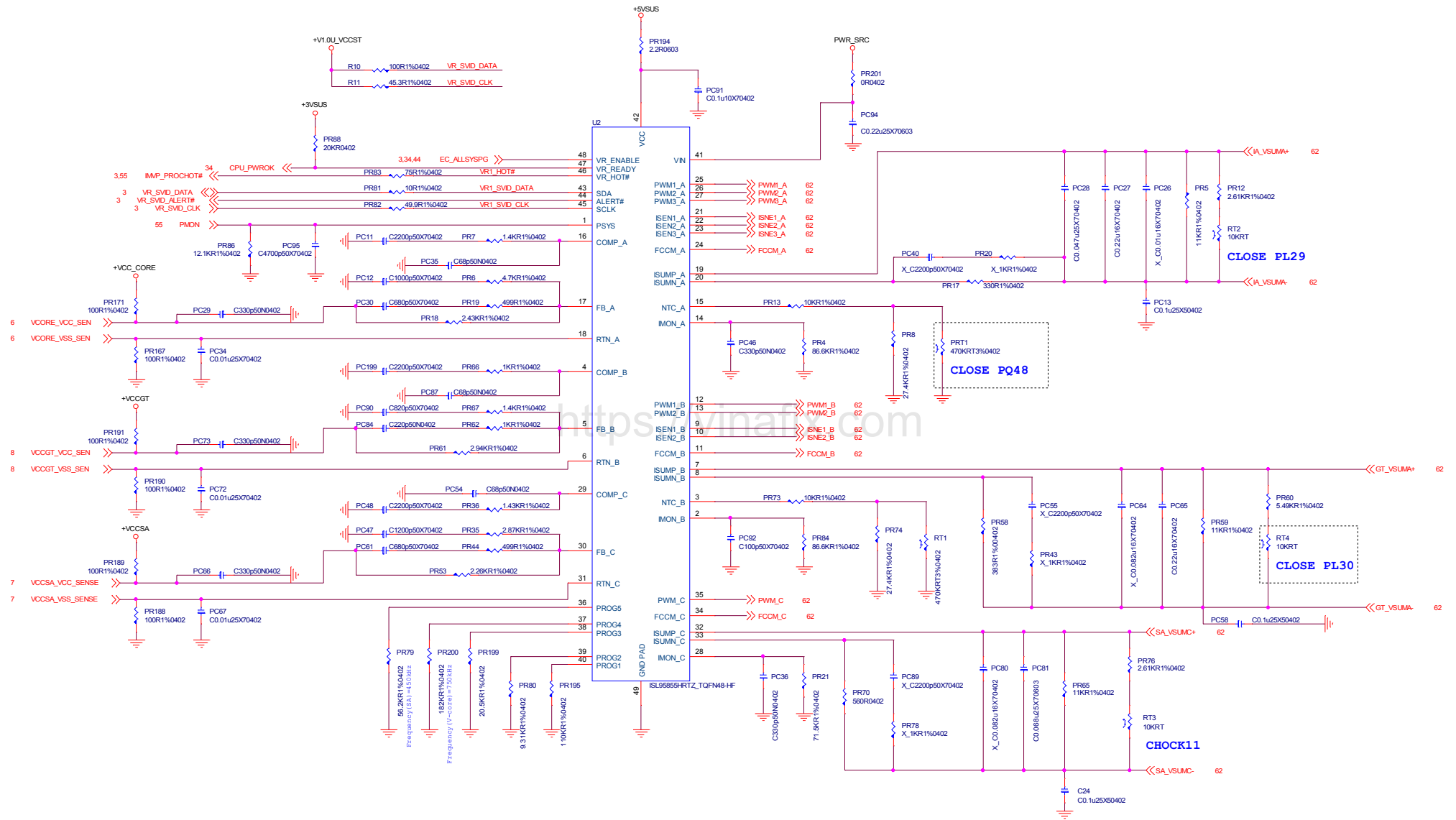
CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

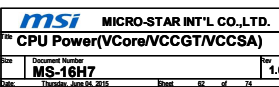
EDP-Peak 130A
EDP-MAX 69A
EDP-Con 65A

0B Change to X7R/1206
1.0 Change to X5R/1206 high



CPU Power IC (ISL95855)





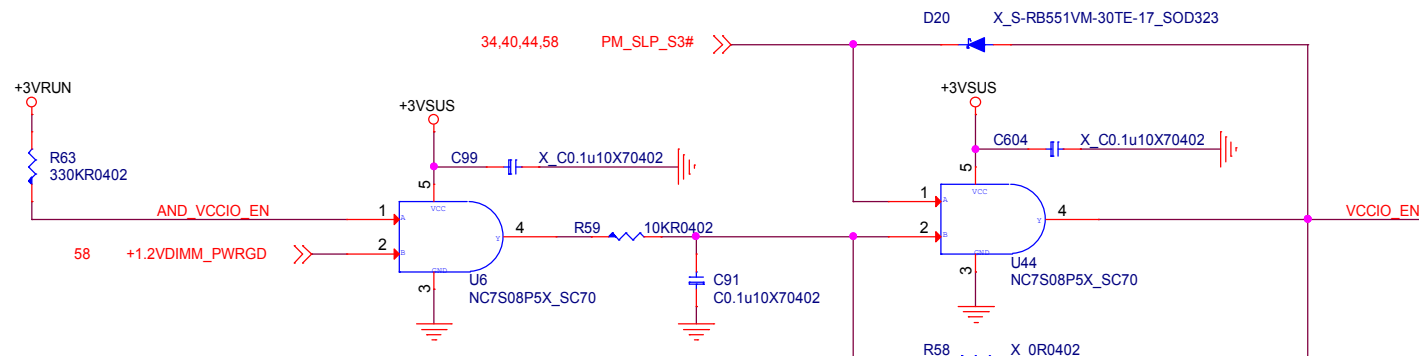
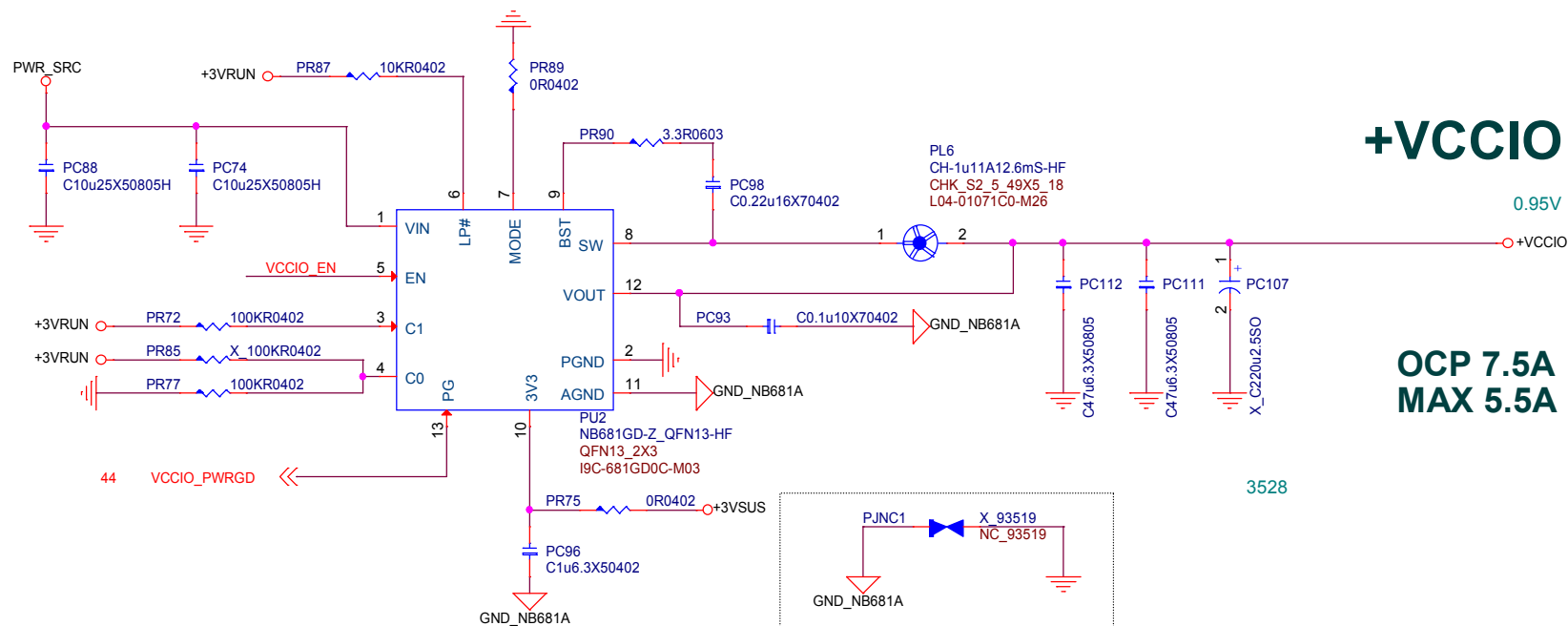
+VCCIO

0.95V

**OCP 7.5A
MAX 5.5A**

3528

<https://vinafix.com>



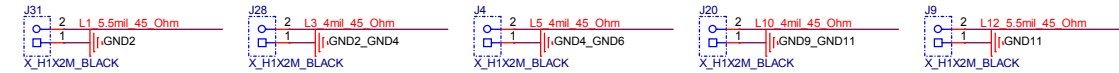
EMI/ Impedence

Impedence Connector No PN

40 ohm



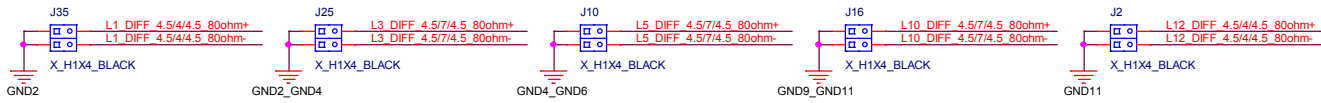
45 ohm



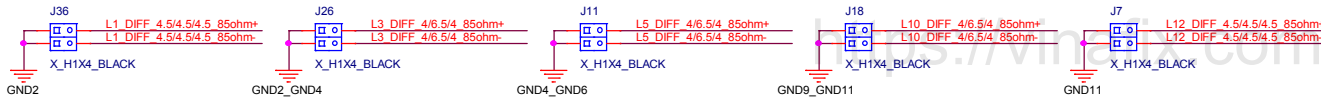
50 ohm



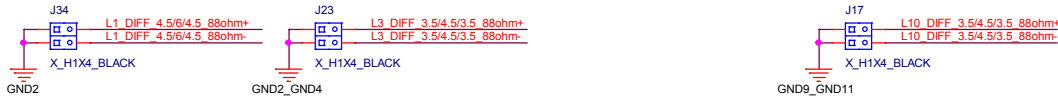
80 ohm



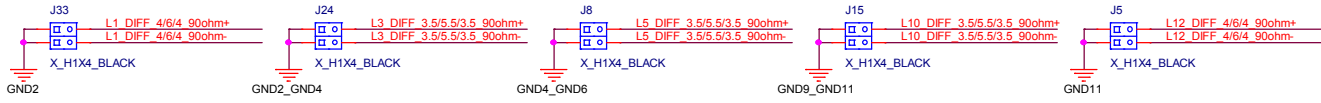
85 ohm



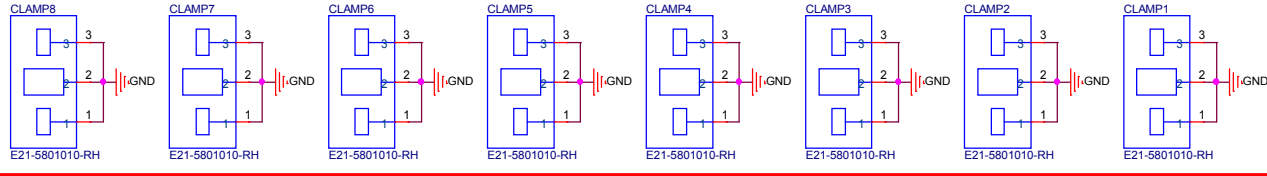
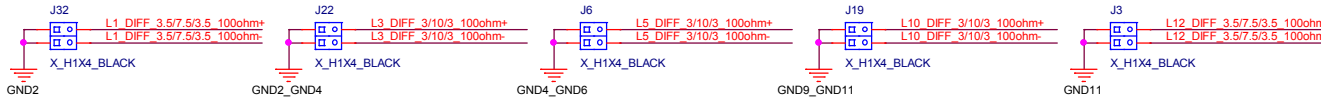
88 ohm



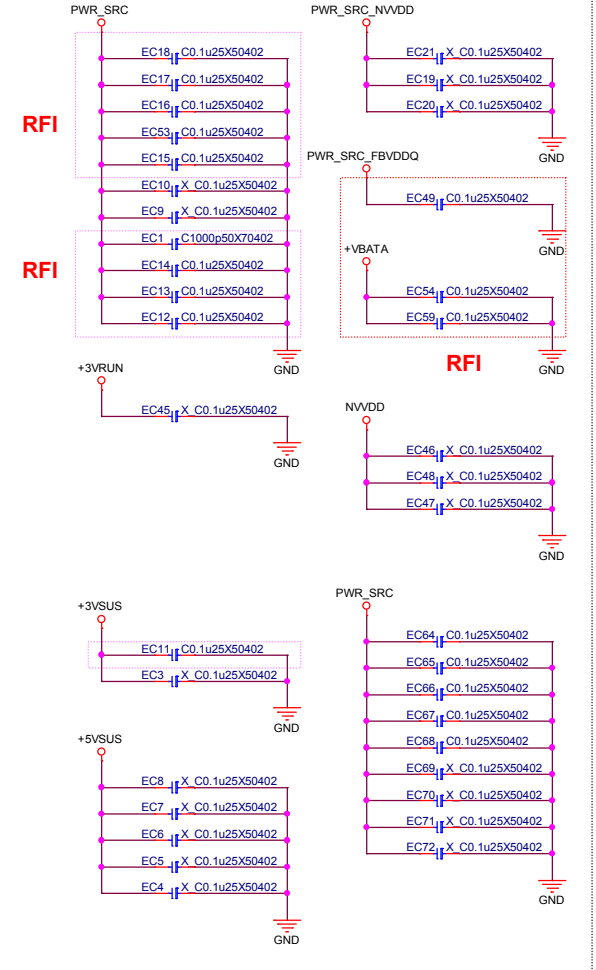
90 ohm



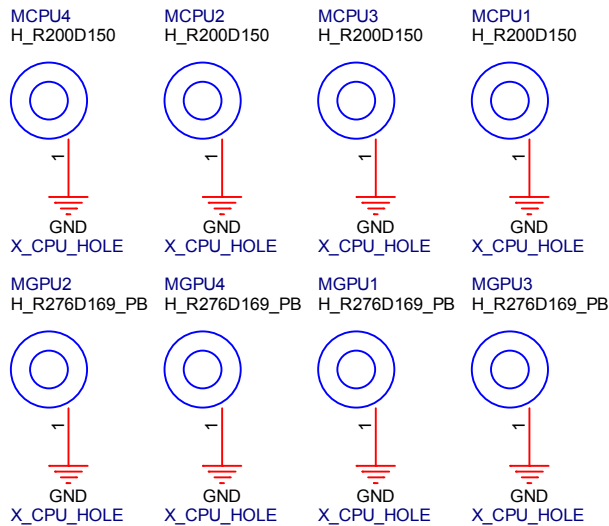
100 ohm



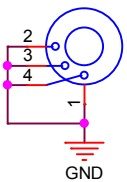
EMI



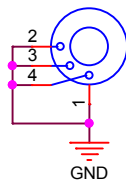
CPU/GPU Holes



M1
X_H_R197D118_PT_V3
H_R197D118_PT_V3

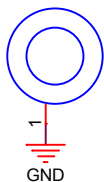


M8
X_H_R197D118_PT_V3
H_R197D118_PT_V3



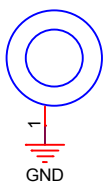
Fan Hole

MH4
H_R197D91
X_ME_SCREW HOLE

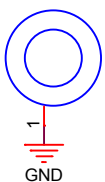


SSD Stand off

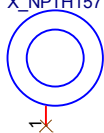
MH2
H_R220D146_PTB
E2B-16H2020



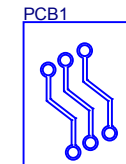
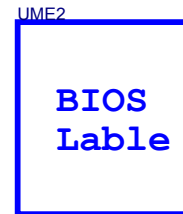
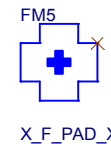
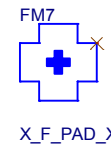
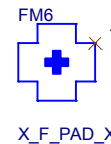
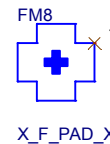
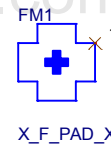
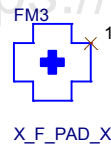
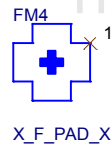
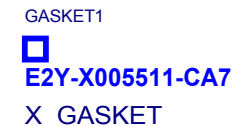
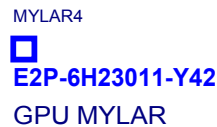
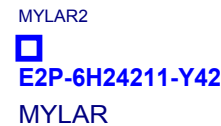
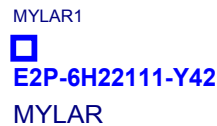
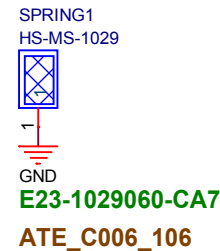
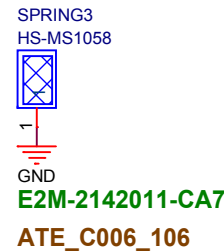
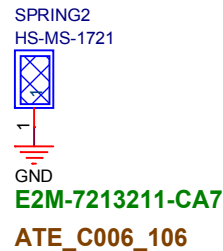
MH1
H_R220D146_PTB
E2B-16H2020



MH3
NPTH157
X_NPTH157



EMI



PF0-16H7110-H73
Hannstar: PF0-16H7110-H73
TRIPOD: PF0-16H7110-T53

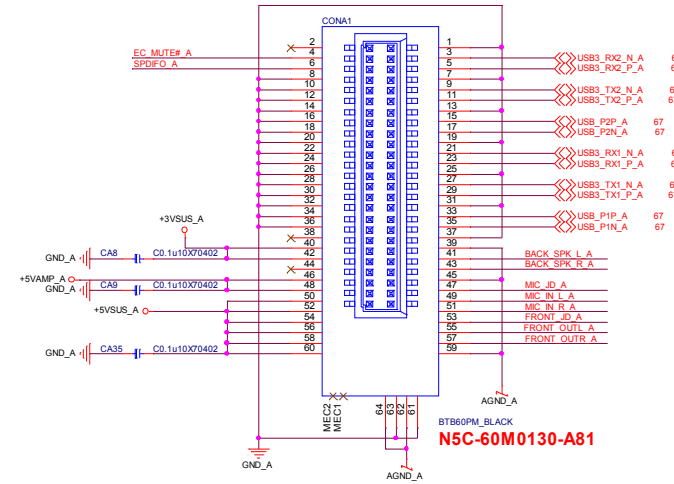
msi

MICRO-STAR INT'L CO.,LTD.

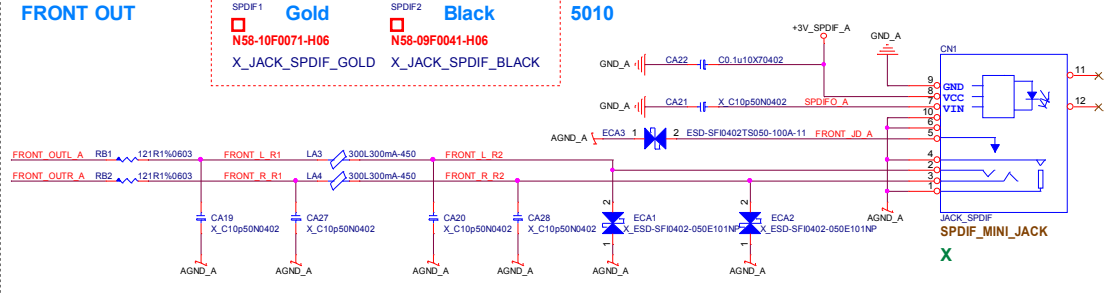
Title		
Screw/ME		
Size	Document Number	Rev
	MS-16H7	1.0
Date:	Thursday, June 04, 2015	Sheet 65 of 74

16H7-A Board (Audio CONN)

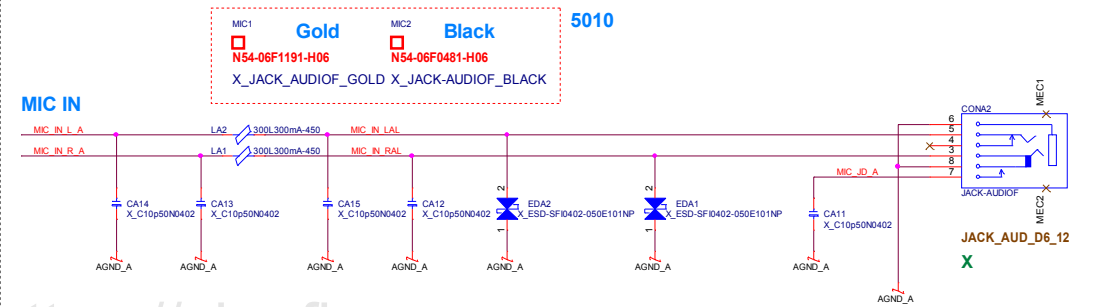
BTB Connector From MB
CONN Pin Current Capability : 0.5A/Pin



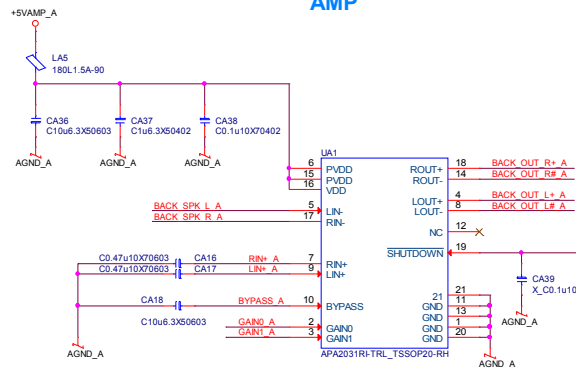
FRONT OUT



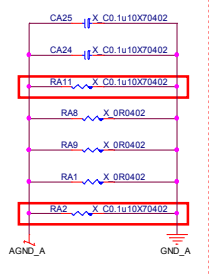
MIC IN



AMP



EMI

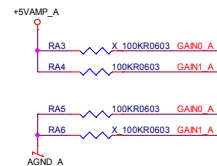


Change to Cap

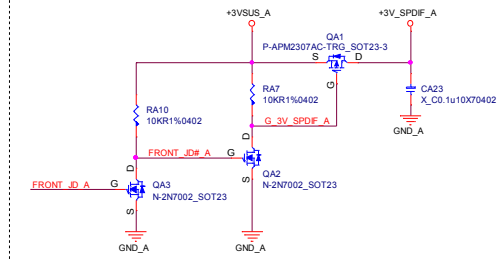
Change to Cap

For APA2031

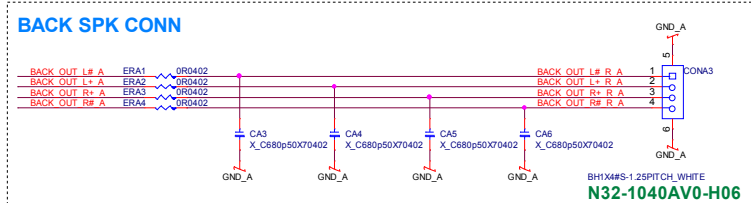
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



SPDIF Power

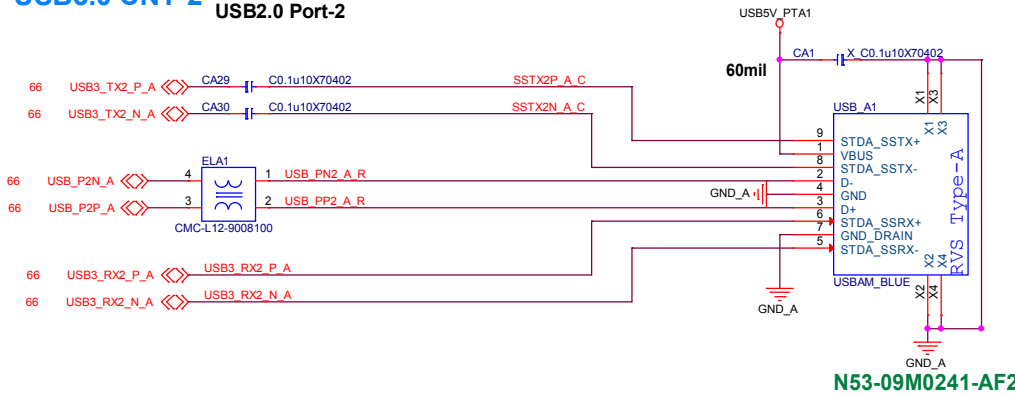


BACK SPK CONN

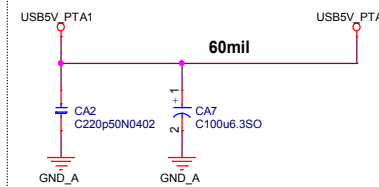


[A] USB3.0 CNT-2/-3

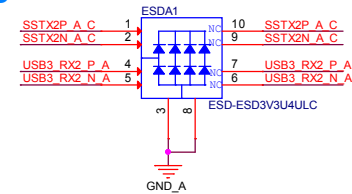
USB3.0 CNT-2 USB3.0 Port-2 USB2.0 Port-2



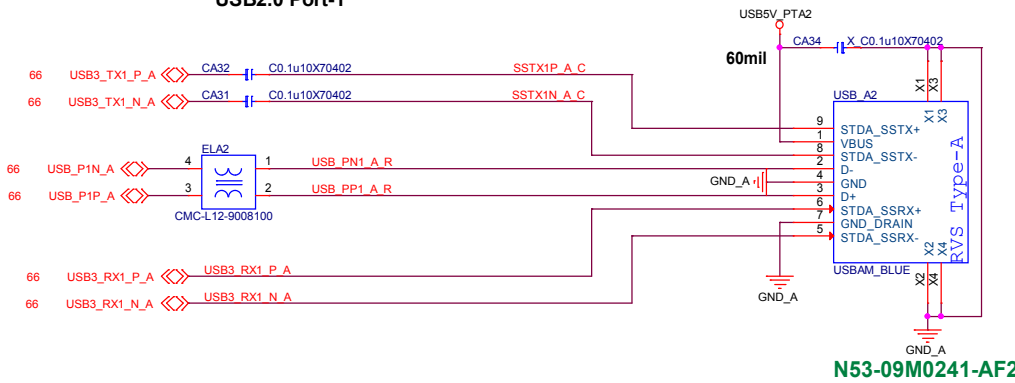
USB Power



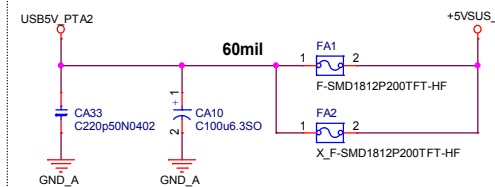
ESD



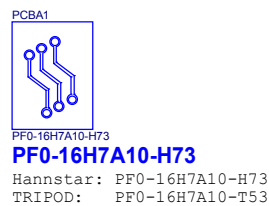
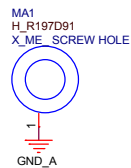
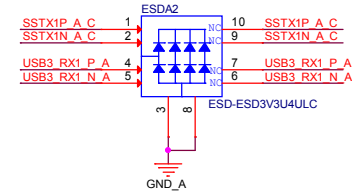
USB3.0 CNT-1 USB3.0 Port-1 USB2.0 Port-1



USB Power



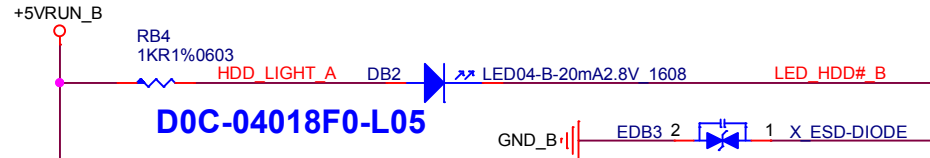
ESD



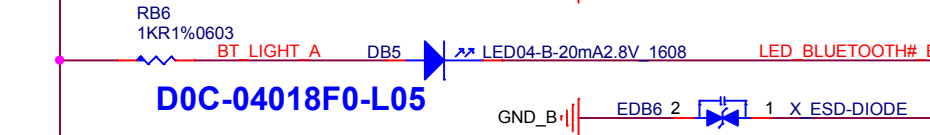
16H7-B Board (LED Board)

LED

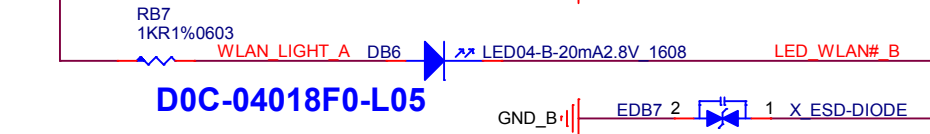
BLUE
(HDD)



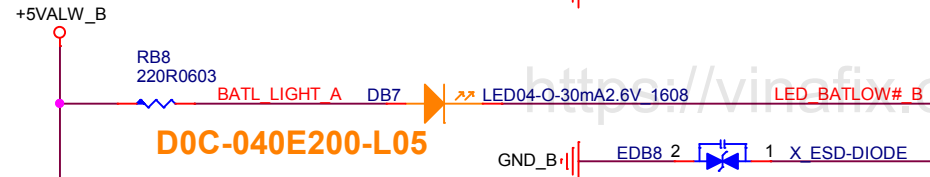
BLUE
(BT)



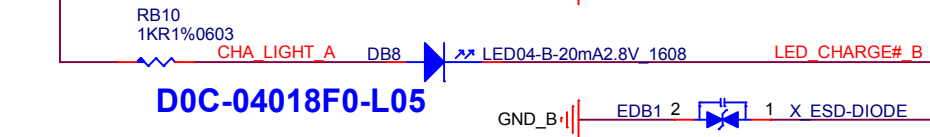
BLUE
(WLAN)



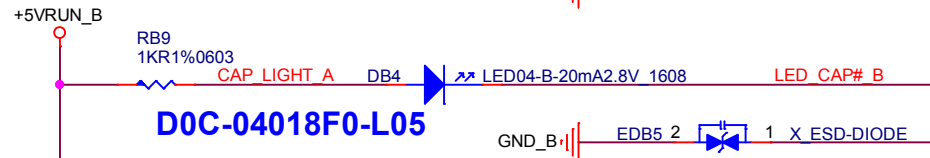
ORANGE
(BATLOW)



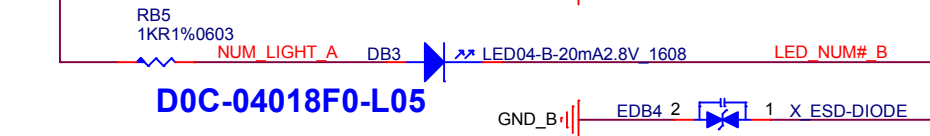
BLUE
(CHARGE)



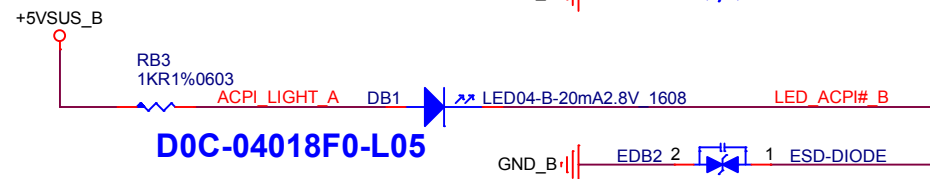
BLUE
(CAP)



BLUE
(NUM)

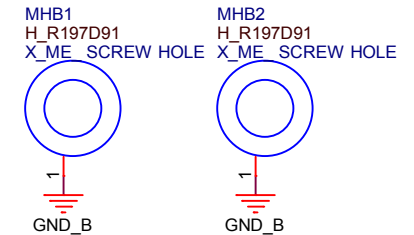
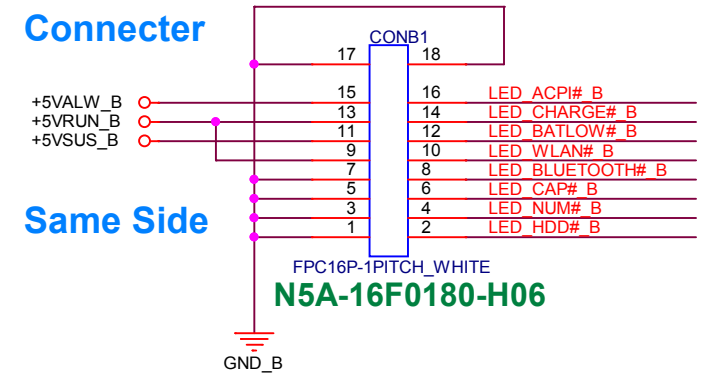


BLUE
(ACPI)

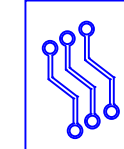


Connector

Same Side



PCBB1

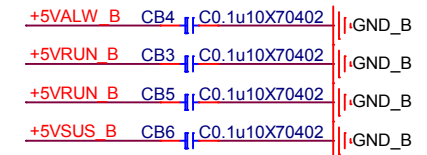


PF0-16H7B10-H73

PF0-16H7B10-H73

Hannstar: PF0-16H7B10-H73

TRIPOD: PF0-16H7B10-T53



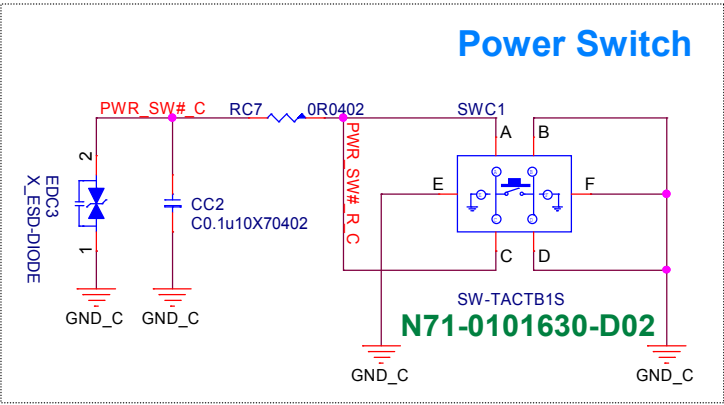
msi

MICRO-STAR INT'L CO.,LTD.

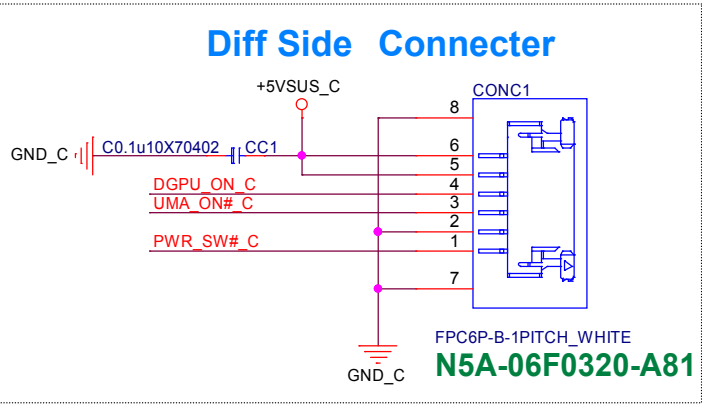
Title			LED Board
Size	Document Number	Rev	
	MS-16H7	1.0	
Date:	Thursday, June 04, 2015	Sheet	68 of 74

16H7-C Board (Power SW Board)

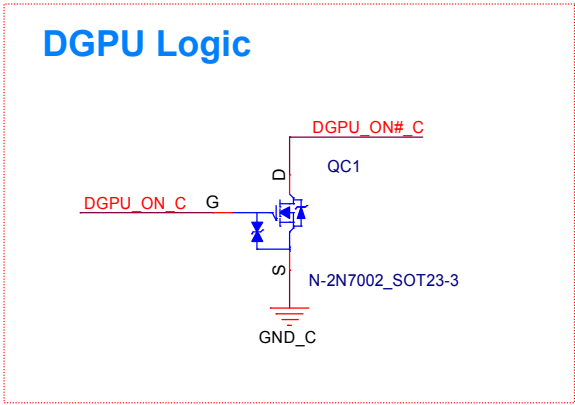
Power Switch



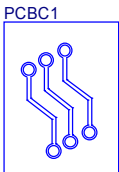
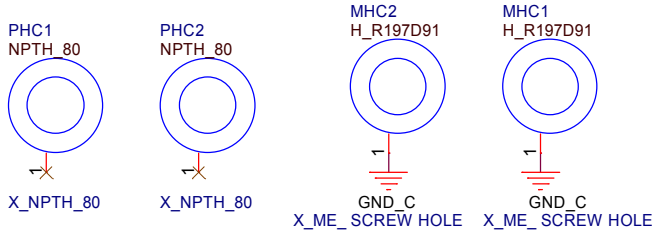
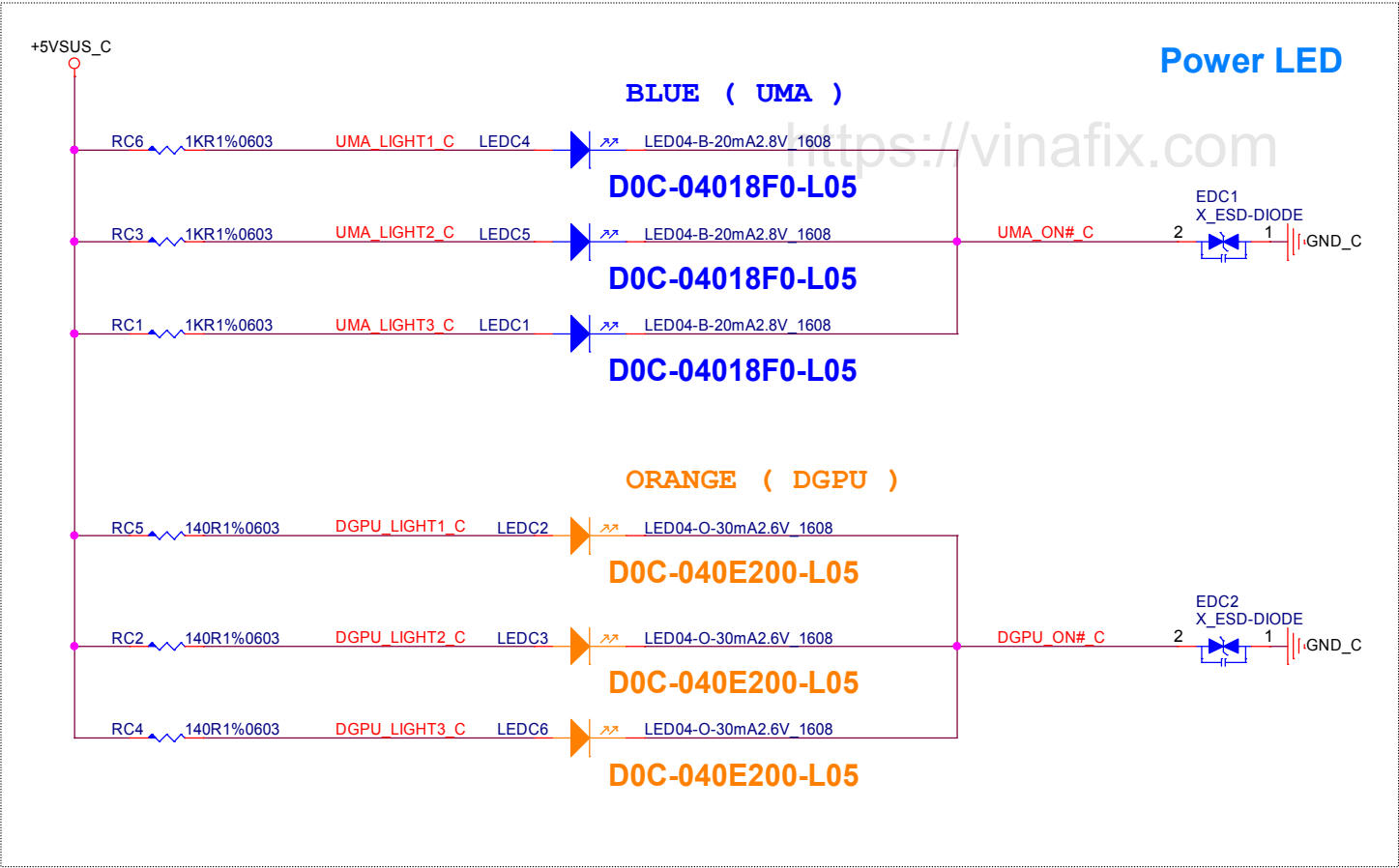
Diff Side Connector



DGPU Logic



Power LED



PF0-16H7C10-H73
PF0-16H7C10-H73
Hannstar: PF0-16H7C10-H73
TRIPOD: PF0-16H7C10-T53

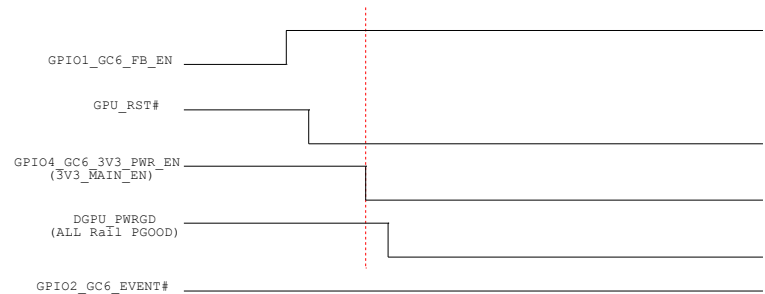


MICRO-STAR INT'L CO.,LTD.

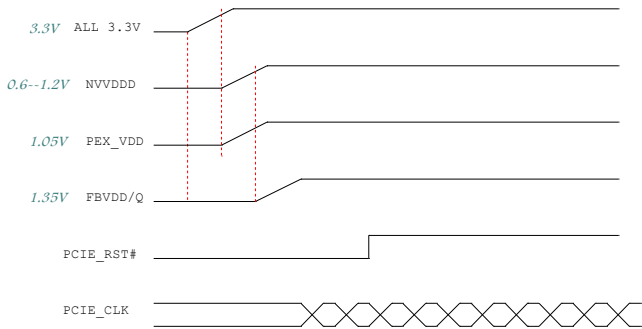
Title		
Power SW Board		
Size	Document Number	Rev
	MS-16H7	1.0
Date: Thursday, June 04, 2015		
Sheet 69 of 74		

MS-16H7 DGPU POWER SEQUENCE

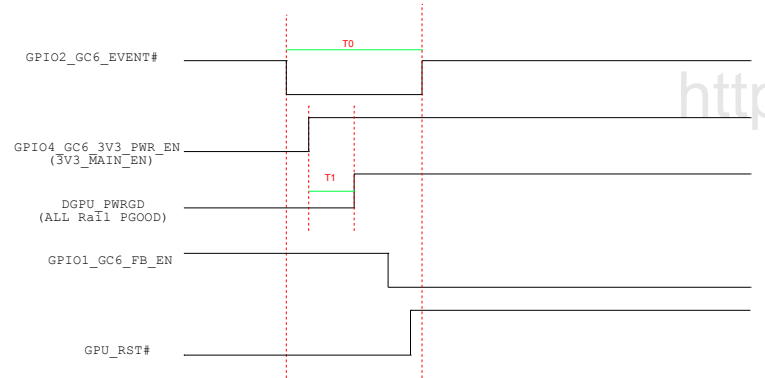
GC6 2.0 ENTRY SEQUENCE



GPU POWER ON SEQUENCE



GC6 2.0 EXIT SEQUENCE



NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltage.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

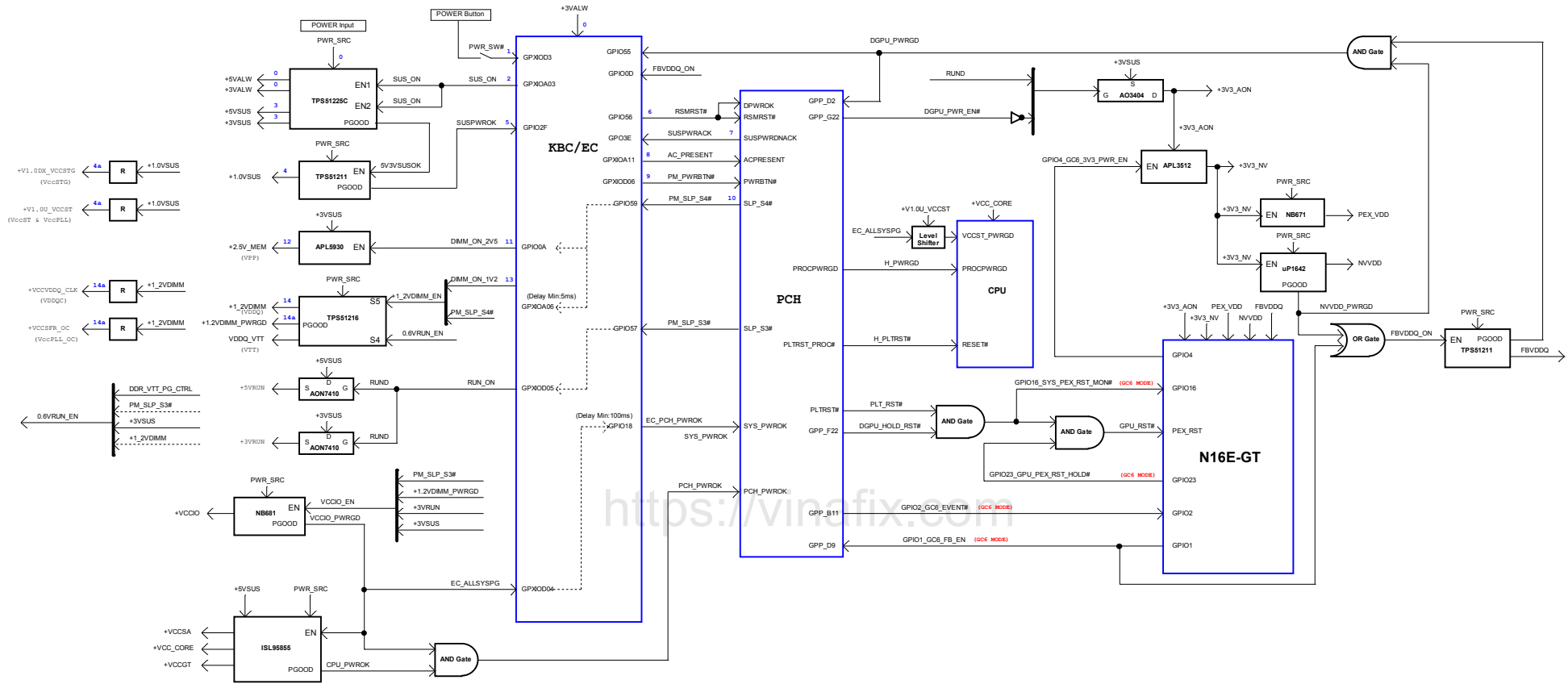
GC6 2.0 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	mS	GPU_EVENT# assertion
T1	0.04	4	mS	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

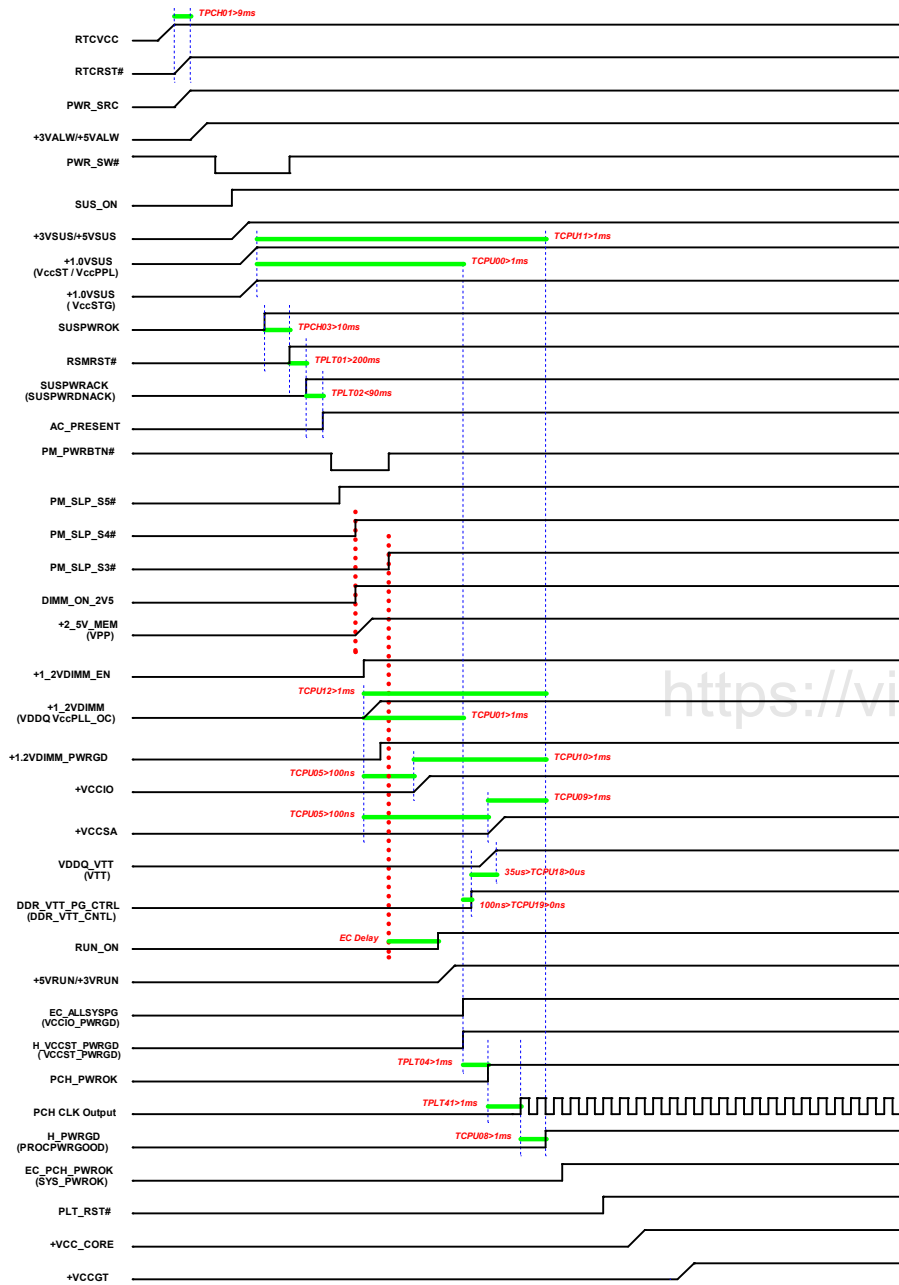
1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

MS-16H7 Power On Block Diagram



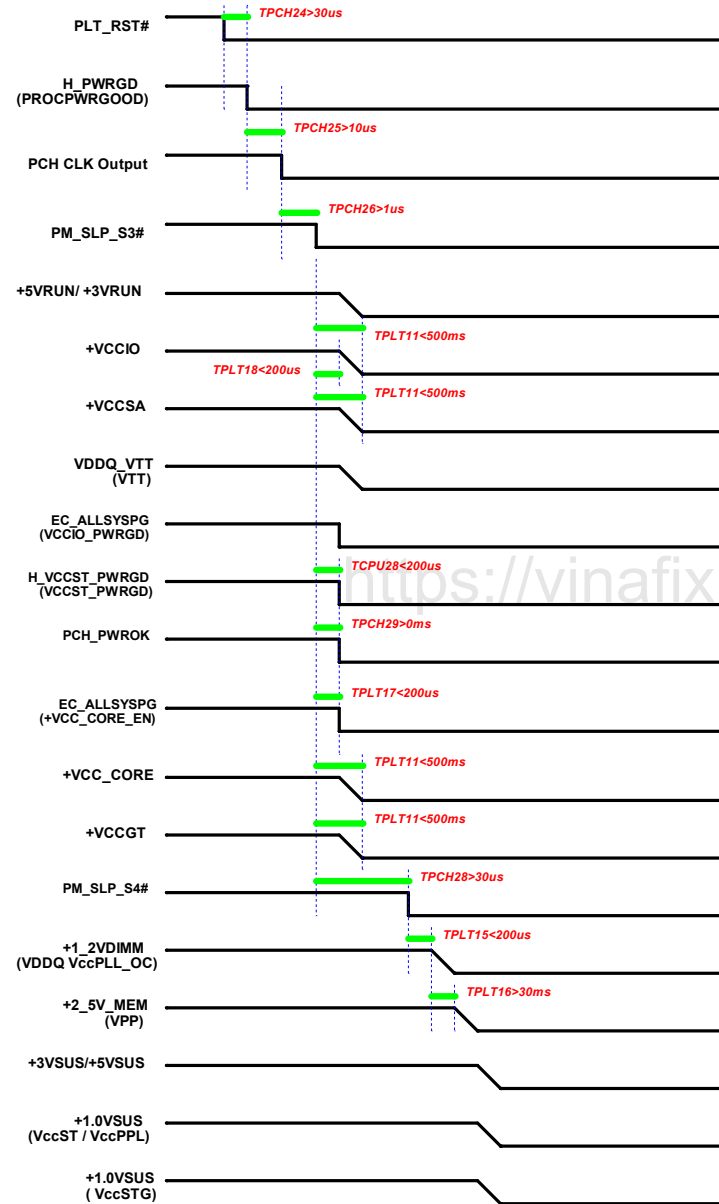
Power On Sequence

G3 -> S0



Power Down Sequence

S0 -> G3



History

1.0: 2015/5/18

- 01. P55 DEL PC148
ADD PR264
- 02 P40 ADD R526
ADD R527
ADD R528
ADD R529
- 03 P41 DEL ESD3
DEL ESD4
DEL ESD5
ADD D4~D18

2015/5/22

- 01. P56 R220 to +3VSUS
R219 to +3VSUS

2015/5/25

- 01. P58 ADD U45
ADD R532
ADD C606
- 02. P63 ADD U44
ADD C604
- 03. P49 U1 PIN29 to GND
- 04. P58 ADD D19
- 05. P63 ADD D20

2015/5/25

- 01. P64 ADD EC64~EC68
ADD EC69~EC72

<https://vinafix.com>



MICRO-STAR INT'L CO.,LTD.

Title		
History		
Size	Document Number	Rev
	MS-16H7	1.0
Date:	Thursday, June 04, 2015	Sheet 74 of 74